CHAPTER 1 Preliminaries

绪论

This book is about linear analog integrated circuits. An analog circuit is qualified as linear if it exhibits a linear relationship between its input and output variables. Regulators, amplifiers, buffers, and filters are typical examples of such circuits. They are used mostly for regulating power supplies, conditioning sensor signals prior to analog-to-digital conversion, or driving an actuator/transducer after digital-to-analog conversion. The last two cases are exemplified in Fig. 1.1 with two simple applications. Figure 1.1(a) shows a voltage amplifier matching up the voltage-mode signal of a temperature-sensing diode to the input range of an analog-to-digital converter (ADC). Figure 1.1(b) shows a transimpedance amplifier converting and filtering the current-mode output signal of a digital-to-analog converter (DAC) into a voltage-mode signal to drive an actuator/transducer load. Both examples exhibit a feature common to almost all linear integrated-circuit applications: Their architecture is in the form of a *closed-loop configuration* consisting of (a) an *operational amplifier* (opamp), and (b) an *external network* built usually with passive components. In a closed-loop configuration, the opamp itself acts as an inaccurate, imprecise, and nonlinear supplier of large voltage gain while the negative feedback provided by the external network trades off the excessive voltage gain for accuracy, precision, and linearity, which are the three fundamental attributes of linear analog signal processing.

Integrated-circuit design in general is a two-stage process. The first stage, called *electrical design*, delivers a complete circuit schematic of the closed-loop configuration annotated with the dimensions and other physical parameters of (a) all external-network components and (b) all opamp internal devices. The second stage, called *physical design*, converts this schematic into an artwork defining the layout to be fabricated. This book is primarily on electrical design; physical design is covered as much as it pertains to electrical design.

Electrical design is a top-down process going through three layers of abstraction as illustrated with a block diagram in Fig. 1.2. Electrical performance of the application, as specified in terms of what we call closed-loop metrics, is the input of the topmost *application layer*. In this layer, design activity begins with the selection of a closed-loop configuration that can handle the application, and moves to the translation of the specified closed-loop metrics into (a) open-loop metrics, which define the target performance of the opamp itself, and (b) external-network device metrics, which define the target performance of external-network components. The intermediate *circuit layer* of design is based on open-loop metrics. Its outcome is twofold: (a) adopting an opamp circuit topology that can satisfy these open-loop metrics, and (b) specifying the target performance of opamp internal devices in terms of device metrics. In the final *device layer* of design, the device metrics specified in application and circuit layers are translated into bias conditions and physical parameters for all opamp devices and external-network components.

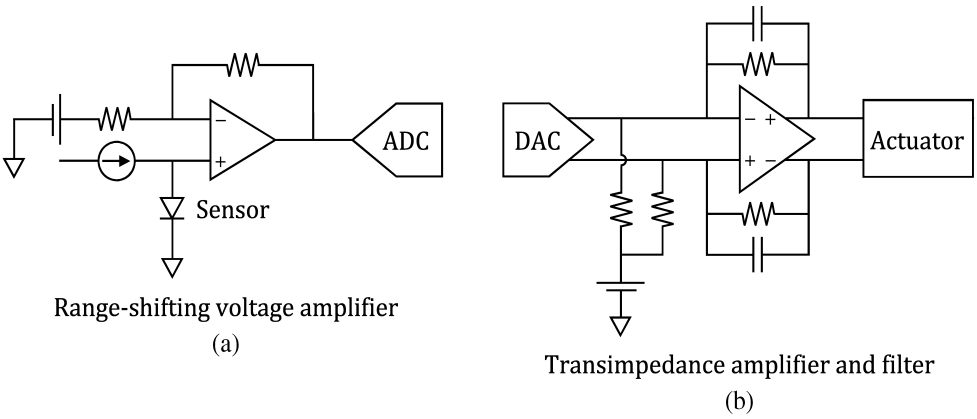

FIGURE 1.1 Two linear integrated-circuit application examples. (a) A single-ended voltage amplifier for conditioning a thermal-sensor signal prior to analog-to-digital conversion. (b) A fully-differential transimpedance amplifier for driving an actuator.

Although the block diagram shown in Fig. 1.2 indicates a one-way flow, it frequently becomes necessary to loop back and redesign as overconstrained or underconstrained design spaces are encountered along the way. However, this does not alter the definitions indicated in Fig. 1.2 for the input metrics or outcomes of any of the three layers.

The main body of this book is divided into three chapters, each dealing with one of the three layers of design. The application layer is covered in Chapter 2. The device layer comes next in Chapter 3. Finally, in Chapter 4, we study the circuit layer and also work on complete linear integrated-circuit design examples involving the contents of the preceding chapters.

The methodology practiced in this book for design and verification is based on Spice simulations, which are run on version-27 of the open-source platform *Ngspice*. The reader is referred to the companion website of this book, www.mhprofessional.com/AICDS, for instructions regarding its download and installation.

Circuit description in Ngspice is based on direct netlist entry whereas commercial simulation platforms generate netlists from schematic entries. Schematic entry is generally faster, easier, and foolproof, which are valuable assets in professional use because they minimize the time and attention needed for circuit description. However, the intricacies of circuit description are better learned by paying attention to details, which is why netlist entry is preferred in this book. Input files describing the netlists of all simulation examples can be downloaded from this book's website. Each of the folders named `chap2`, `chap3`, and `chap4` contains the files used in one particular chapter. The first step of running a simulation with any of these files is to open the Ngspice executable. Next, the folder containing the input file is defined as the current directory if it is not already so. For a file residing in, for example, `c:\spice\chap3` of an MS Windows installation, this is done by entering

```
cd c:\spice\chap3
```

at the prompt as shown at the top of Fig. 1.3. Next, the filename itself is entered as exemplified in the middle part of Fig. 1.3 for an input file `ex3-16.sp`. Finally, entering the command `run` as shown at the bottom of Fig. 1.3 initiates the simulation. As the

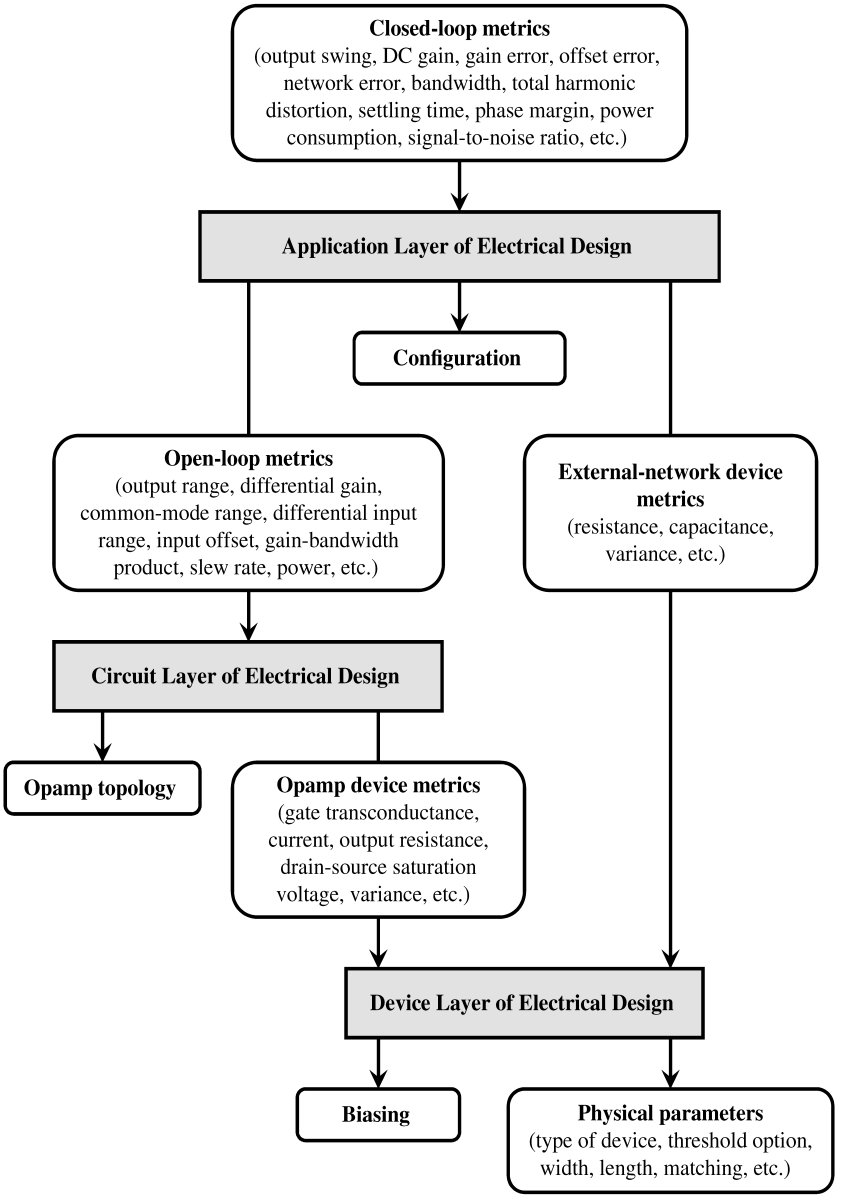

FIGURE 1.2 Layers of abstraction in electrical design.

reader will experience initially in Example 2.9 of Subsection 2.4.2, it is possible to start a simulation without entering a `run` command provided that the input file is properly scripted. As to reading out or plotting the outcomes of a simulation, the reader will find the necessary descriptions inside the examples presented throughout the following three chapters.

Input files are prepared with a text editor, and saved with extension `.sp`. Each begins with a title line and ends with a `.end` line. The lines in between are expected to describe

FIGURE 1.3 Screenshots showing the steps of running an input file in an MS Windows installation. *Top:* Changing the directory. *Middle:* Declaring the filename. *Bottom:* Initiating the simulation.

at least the network of components, their parameters, and the type of analysis to be performed. For an example, the reader is referred to file `ex2-1.sp`, which netlists the circuit schematic shown in Fig. 2.5. Its line-by-line description is as follows:

Line 1 Filename is typed in the title line. Since Spice does not consider this line as a declaration, any text can be included without affecting the outcome of the simulation.

Line 2 This line quantifies certain parameters. Typographically, it spans over two lines as indicated by the plus sign appearing at the beginning of the extension. This is how a long line can be accommodated in an input file.

Line 3 Another file `opmacro1.sp` is called by this line. This additional file actually describes the netlist of the opamp `x1` declared in line 4 as a *subcircuit*. If a circuit is involved in multiple simulations, or multiple instances of a circuit are involved in a simulation, we prefer to describe such a circuit as a subcircuit and simply include its instances whenever or wherever needed.

Line 4 This is an element line where an instance of the subcircuit `opamp` is called. Note that a subcircuit instance is identified with a name beginning with `x`. The three numbers appearing after the name are the node numbers of the top-level circuit in which the subcircuit is embedded.

Lines 5 and 6 These lines begin with `r`, and therefore describe the instances of resistors. Each contains two node identifiers and the value of the resistance.

Lines 7 and 8 Independent voltage sources are defined in these lines. They begin with `v`, and continue with two node identifiers. The first between the two is the reference node. The third number `0.54` appearing in line 7 is the voltage imposed onto the reference node with respect to the ground node. Note that 0 is the universal identifier of ground node. The voltage of the source `vd` is undefined in line 8 because it is changed as a part of the analysis defined next in line 9.

Line 9 Beginning with a dot, this line describes a command. Specifically, it defines a dc simulation as indicated by `.dc`. The voltage of the independent source `vd` is the variable of this simulation. It varies between 0.476 and 0.723 V in 1-mV increments.

The end of the input file is declared in the very last line.

Although the examples included in the following chapters will help the reader master the basics of simulation with Ngspice, it will be much more beneficial at this stage to read the specific sections of the user manual, which is included in the downloaded Ngspice package.

CHAPTER 2 Application Layer
应用层面

2.1 Introduction 引言

As stated in Chapter 1, the application layer of electrical design involves (a) selection of an appropriate closed-loop configuration for the application, and (b) translation of the specified closed-loop metrics into open-loop metrics for the opamp and device metrics for the external network. Available closed-loop amplifier configurations are well documented in related literature. No attempt is made in this book to present their inventory but most popular configurations are presented in examples throughout this chapter. The main emphasis of the chapter is on the analytical techniques and tools used in translating closed-loop metrics into open-loop metrics and external-network device metrics. These techniques and tools are generalized into four major architectural classes depending on (a) whether amplification is performed in continuous time or in discrete time, and (b) whether signal representation is single ended or fully differential. The case of continuous-time/single-ended amplifier configurations, being the most fundamental of the four, is covered in the first nine sections of this chapter. Based on the foundation thus established, coverage is then extended to continuous-time/fully-differential configurations in Section 2.10, to discrete-time/single-ended configurations in Section 2.11, and finally to discrete-time/fully-differential configurations in Section 2.12.

Most of the concepts presented in this chapter are supported with Spice simulations conducted with a parameterized single-ended or fully-differential opamp macromodel defined as a subcircuit. The single-ended version is netlisted in the input file `opmacro1.sp`. As shown in Fig. 2.1(a), this macro interfaces with the closed-loop configuration through the following three pins:

1. `ninv`: Noninverting input.
2. `inv`: Inverting input.
3. `out`: Output.

The user-defined parameters of the single-ended opamp macro are described in the following list for future reference.

- `vdd`: Positive power-supply voltage. Introduced in Subsection 2.2.1.
- `vss`: Negative power-supply voltage (zero for a single-supply opamp). Introduced in Subsection 2.2.1.
- `voh`: Higher limit V_{OH} of output range. Introduced in Subsection 2.2.1.

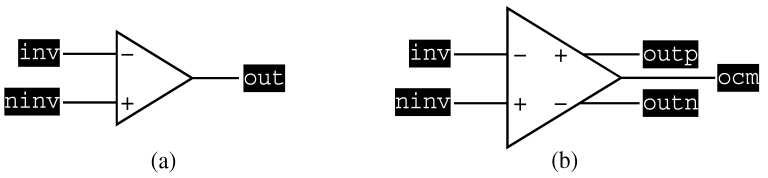

FIGURE 2.1 Symbols and pin configurations of the opamp macromodels defined as subcircuits. (a) Single-ended `opmacro1.sp`. (b) Fully-differential `opmacro2.sp`.

- `vol`: Lower limit V_{OL} of output range. Introduced in Subsection 2.2.1.
- `a0`: DC differential gain A_0 at the midpoint of the output range. Introduced in Subsection 2.4.1.
- `fgbw`: Gain-bandwidth product f_{GBW}. Introduced in Subsection 2.5.1.
- `vdir`: Differential-input range V_{DIR}. Introduced in Subsection 2.5.2.
- `fnd`: Nondominant pole frequency f_{nd}. Introduced in Section 2.7.
- `vos` at `vout`: Offset voltage V_{os} defined at an output bias voltage V_O. Introduced in Subsection 2.4.1. Unlike the preceding parameters, these two are set by default to `vos= 0` and `vout= (voh+vol)/2` but can be reset by adding the following lines to the main input file that contains the opamp subcircuit `opmacro1.sp`:

```
.control
alter v.<subcircuit identifier>.vos=<value>
alter v.<subcircuit identifier>.vout=<value>
.endc
```

  where `<subcircuit identifier>` is the name of the opamp instance, such as `x1`, and `<value>` is the reset value.

The input file netlisting the fully-differential opamp macro is `opmacro2.sp`. As shown in Fig. 2.1(b), this macro interfaces with the closed-loop configuration through the following five pins:

1. `ninv`: Noninverting input.
2. `inv`: Inverting input.
3. `outp`: Noninverting output. Described in Subsection 2.10.1.
4. `outn`: Inverting output. Described in Subsection 2.10.1.
5. `ocm`: This is the pin where the output common-mode voltage V_{OCM} is externally applied as described in Subsection 2.10.1.

The user-defined parameters of the single-ended opamp macro described previously apply also to this opamp with one exception. The exception is the replacement of the single-ended open-loop dc gain parameter `a0` with the differential open-loop dc gain parameter `adif0` which is defined in Subsection 2.10.3.

Another adjustable opamp parameter is the offset voltage `vos`, whose default value is zero. The user may alter it by adding the following line to the main input file containing the opamp subcircuit `opmacro2.sp`:

```
.control
alter v.<subcircuit identifier>.vos=<value>
.endc
```

where `<subcircuit identifier>` is the name of the opamp instance, such as `x1`, and `<value>` is the reset value. The offset voltage of a fully-differential opamp is described in Subsection 2.10.3.

2.2 First-Order DC Response 一阶直流响应

DC response is of prime importance in design because most applications operate with dc bias and are supposed to handle signals whose frequency spectra include dc. Furthermore, a closed-loop configuration treats a time-varying signal not much differently than a pure dc as long as its bandwidth is wider than the frequency spectrum of the signal. The voltage amplifier shown in Fig. 1.1(a) is a good example. It is biased with a dc voltage as well as a dc current, and is driven by a signal of thermal origin which usually remains constant for most of the time and varies slowly otherwise.

In this section, we present an analysis of closed-loop dc response using an ideal opamp model based on the so-called *virtual-short approximation*. Despite its ultimate simplicity, the model is still sufficiently accurate for specifying the resistive components of the external network and open-loop dc range metrics of the opamp. In some applications, the designer has to consider also the second-order features of closed-loop dc response. Those are discussed in Section 2.4 on the basis of a more accurate opamp model.

2.2.1 First-Order Open-Loop DC Transfer Characteristic and Range Limitations 一阶开环直流传输特性和量程限制

Shown in Fig. 2.2(a) is the symbol convention we generally use for opamp terminal voltages regardless of the type of response being analyzed. v_O is the total instantaneous output voltage. v_{IN} and v_{IP} represent the total instantaneous voltages of the inverting and noninverting input terminals, respectively. In steady state, the opamp does not draw any dc current from these input terminals because they are capacitively terminated inside the opamp. All of these voltages are defined with respect to system ground. The difference between the two input voltages, as defined by

$$v_{ID} \doteq v_{IP} - v_{IN}, \tag{2.1}$$

is called *differential-input voltage*. The average of the two defined by

$$v_{CM} \doteq \frac{v_{IP} + v_{IN}}{2} \tag{2.2}$$

is called *common-mode voltage*.

In this book, the relationship imposed by the opamp between v_O and v_{ID} is generally called *open-loop transfer function* if expressed analytically, or *open-loop transfer characteristic* if displayed graphically. The dc form of the open-loop transfer characteristic is shown in Fig. 2.2(b) for an ideal single-supply opamp powered by a positive supply-voltage V_{DD} with respect to system ground. The ideal features of the characteristic are associated with its segment located between the two output-voltage levels $v_O = V_{OL}$ and $v_O = V_{OH}$. In a

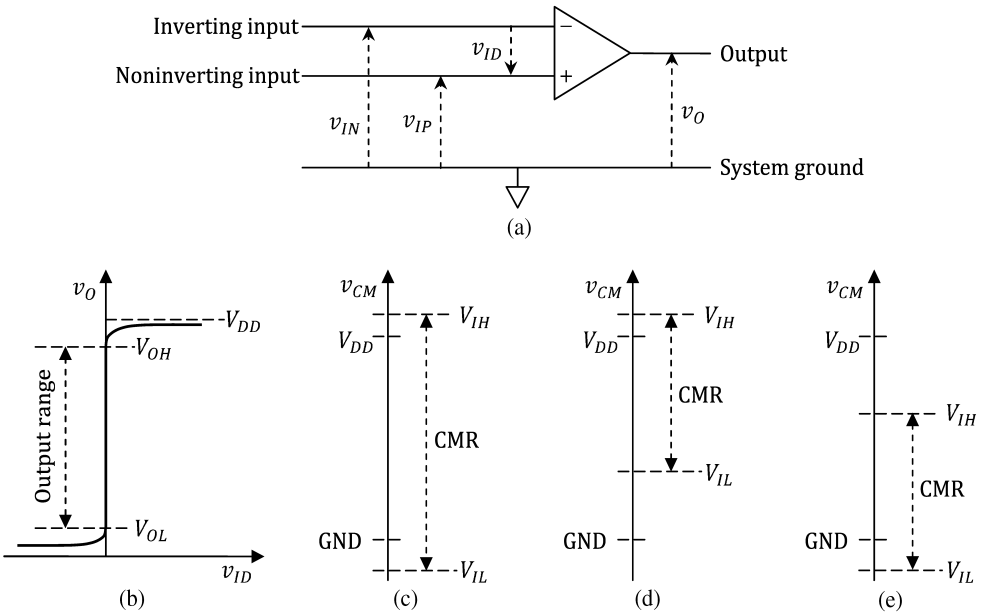

FIGURE 2.2 (a) Symbol convention for opamp input and output variables. (b) Open-loop dc transfer characteristic and output range in an ideal single-supply opamp. (c) A rail-to-rail common-mode range. (d) A common-mode range excluding ground. (e) A common-mode range excluding the supply voltage V_{DD}.

real opamp, this segment is nonlinear with a large but finite and varying slope as will be discussed in detail in Section 2.4. In first-order dc modeling, we assume it to be perfectly vertical and located at

$$v_{ID} = 0. \tag{2.3}$$

When functioning properly, the negative feedback established by the external network of the closed-loop configuration keeps the operation point of the opamp on this ideally vertical segment. The range between V_{OL} and V_{OH} is an open-loop metric called *output range*. It must be made wide enough by design to safely accommodate the so-called *output swing*, which is a closed-loop metric defined as the range in which v_O is expected to vary. This design constraint can be stated as

$$V_{OL} < V_{O(\min)}, \tag{2.4}$$

and

$$V_{OH} > V_{O(\max)}, \tag{2.5}$$

where $V_{O(\min)}$ and $V_{O(\max)}$ are the limits of the output swing.

According to (2.1) and (2.2), the common-mode voltage of an ideal opamp complying with (2.3) is given by

$$v_{CM} = v_{IP} = v_{IN}, \tag{2.6}$$

which enables us to interpret the common-mode voltage as the common value of the identical v_{IP} and v_{IN}. Ideally, an opamp is expected to be insensitive to v_{CM}, that is, v_O should remain unchanged even when v_{IP} and v_{IN} commonly change in time. In reality, all opamps are somewhat sensitive to v_{CM}, but the sensitivity is, to a first-order approximation, negligible as long as v_{CM} remains within a particular range known as *common-mode range* (CMR). This range is an open-loop metric. It must be made sufficiently wide by design to accommodate the minimum and maximum values $V_{CM(\min)}$ and $V_{CM(\max)}$ of the common-mode voltage. Representing the lower and upper limits of CMR with V_{IL} and V_{IH}, this design constraint can be expressed with

$$V_{IL} < V_{CM(\min)}, \tag{2.7}$$

and

$$V_{IH} > V_{CM(\max)}. \tag{2.8}$$

The range $V_{CM(\min)} \leq v_{CM} \leq V_{CM(\max)}$ is called *common-mode swing* in this book. It is a closed-loop metric.

Depending on the topology of the opamp, V_{IL} may be lower or higher than ground. Likewise, V_{IH} may be lower or higher than V_{DD}. If CMR includes both ground and V_{DD}, as shown in Fig. 2.2(c), the opamp is said to have a *rail-to-rail input*. Yet, some other topologies offer a CMR excluding ground or V_{DD}, as depicted in Figs. 2.2(d) and (e), respectively.

In the past, amplifiers used to be built mostly with *split-supply* opamps which are powered symmetrically by a positive supply V_{DD} and a negative supply V_{SS}. The main benefit of split-supply powering is that it enables an amplifier to handle bipolar signals[1] without necessitating any bias. Over the years, however, the diversification of signal-processing applications has introduced many other forms of signals which can't be processed without bias anyway. More importantly, the cost of incorporating two separate power supplies is prohibitively high for the rapidly expanding application area of battery-operated portable equipment. These trends have diminished the popularity of split-supply opamps. Still, it is worth knowing that the only effect the split-supply scheme has on the first-order open-loop dc transfer characteristic is to shift it down as shown in Fig. 2.3(a). Since the output range now includes $v_O = 0$, the opamp can put out a signal centered around the ground. As shown in Figs. 2.3(b) to (d), the CMR also shifts down to include the ground, which is why a split-supply opamp can also handle a common-mode signal swinging around ground.

2.2.2 DC Analysis with Virtual-Short Approximation 基于虚短近似的直流分析

In order to specify V_{IL} and V_{IH} of the common-mode range and V_{OL} and V_{OH} of the output range for a given application, one has to determine first the limits $V_{CM(\min)}$ and $V_{CM(\max)}$ of the common-mode swing and $V_{O(\min)}$ and $V_{O(\max)}$ of the output swing. In many cases, the limits of the output swing are readily available from closed-loop specifications. In other cases, they need to be determined from a dc analysis of the closed-loop configuration. The limits of the common-mode swing are also derived from the same analysis. A simple first-order analysis based on (2.3) is deemed sufficient for this purpose despite its

[1] Swinging symmetrically around ground.

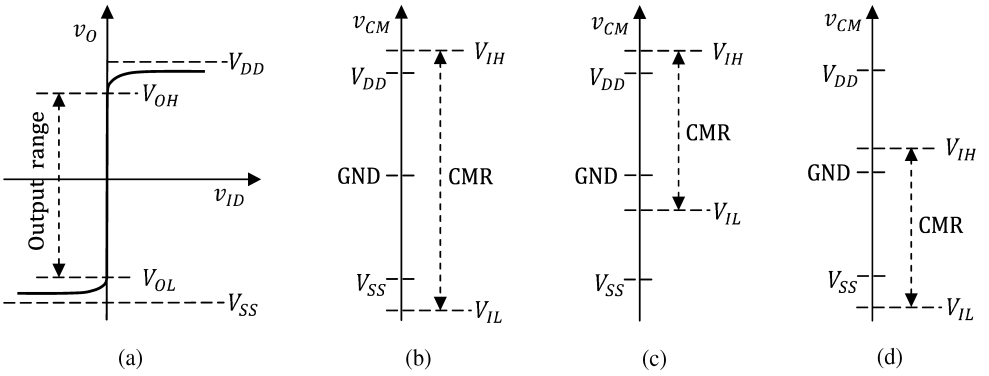

FIGURE 2.3 DC range metrics in an ideal split-supply opamp. (a) Open-loop dc transfer characteristic and output range. (b) A rail-to-rail common-mode range. (c) A common-mode range excluding the negative supply voltage V_{SS}. (d) A common-mode range excluding the positive supply voltage V_{DD}.

inaccuracies because the safety margins by which these dc range metrics are quantified from (2.4), (2.5), (2.7), and (2.8) are reasonably wide anyway.

Known as *virtual-short approximation*, (2.3) enables us to relate v_O and v_{CM} to the input variables of a closed-loop configuration directly from the external network while treating the opamp as an instrument that virtually equates v_{IN} to v_{IP}. The following examples introduce the reader to its use in first-order dc closed-loop analysis and in specifying open-loop dc range metrics.

Example 2.1 An annotated schematic of the temperature-sensor application of Fig. 1.1(a) is shown in Fig. 2.4(a). It is built with a 1.8-V single-supply opamp, a sensor diode biased by a dc current I, and a feedback network comprising a bias source V_B and resistors R_1 and R_2. This closed-loop configuration is expected to amplify and shift the temperature-dependent voltage v_D of the sensor diode into an output swing between $V_{O(\min)} = 0.150$ V and $V_{O(\max)} = 1.650$ V corresponding to the temperature range $-40°\text{C} \le T \le 125°\text{C}$. The voltage v_D across the diode equals $V_D = 626$ mV at $T = 25°$C, and exhibits a temperature sensitivity $\theta \doteq \partial v_D/\partial T = -1.5$ mV/°C within the specified temperature range. We will

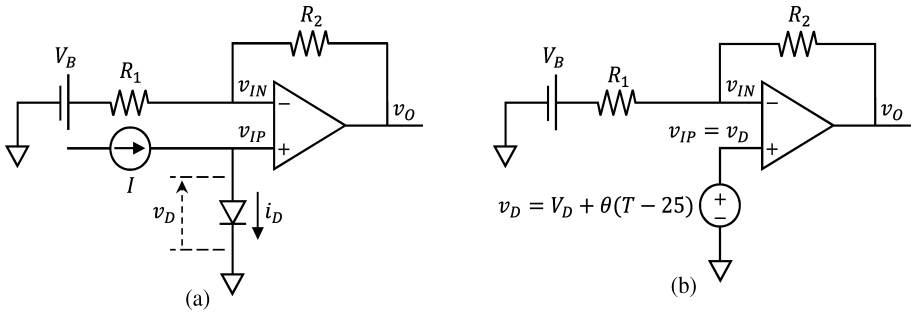

FIGURE 2.4 (a) Annotated schematic of the temperature-sensor application. (b) Equivalent circuit.

determine (a) R_2/R_1 and V_B for the external network, and (b) the limits of output range and common-mode range for the opamp.

Work The sensor diode and its bias current source I can be represented with a single dc voltage source v_D modeled by

$$v_D = V_D + \theta(T - 25)$$

and shown in Fig. 2.4(b). Considering the specified values of V_D, θ, and T, we identify the following range for v_D:

$$0.476\,\text{V} \le v_D \le 0.723\,\text{V}. \tag{2.9}$$

We now analyze the closed-loop configuration shown in Fig. 2.4(b) with a view to determining the relationship between its output voltage v_O and input variables V_B and v_D. This relationship will be used for specifying the dc range specifications and design constraints. Note that the analytical relationship between the output voltage and input variables of a closed-loop configuration is generally called *closed-loop transfer function* in this book. For all linear configurations, it assumes the form

$$v_O = \sum_{j=1}^{n} A_{cl,j} x_j, \tag{2.10}$$

where x_j, $j = 1, \ldots, n$ are the input variables of the configuration, and $A_{cl,j}$ is the *closed-loop gain* for input variable x_j.

Let's begin with the observation $v_{IP} = v_D$ in Fig. 2.4(b). Since $v_{IN} = v_{IP}$ due to virtual short, we therefore write

$$v_{IN} = v_D. \tag{2.11}$$

Additionally, the currents flowing in R_1 and R_2 are identical, hence

$$\frac{v_{IN} - V_B}{R_1} = \frac{v_O - v_{IN}}{R_2}. \tag{2.12}$$

Canceling v_{IN} between (2.11) and (2.12) and solving for v_O, we obtain the following first-order dc transfer function of the closed-loop configuration

$$v_O = \left(1 + \frac{R_2}{R_1}\right) v_D - \frac{R_2}{R_1} V_B, \tag{2.13}$$

which indeed complies with the general form (2.10), and indicates $A_{cl,D} = 1 + (R_2/R_1)$ for v_D and $A_{cl,B} = -R_2/R_1$ for V_B.

We now use (2.13) for determining the external-network device metrics R_2/R_1 and V_B. To this end, we rewrite this equation once for $v_O = V_{O(\text{min})} = 0.150$ V and $v_D = V_{D(\text{min})} = 0.476$ V, and next for $v_O = V_{O(\text{max})} = 1.650$ V and $v_D = V_{D(\text{max})} = 0.723$ V. Only V_B and R_2/R_1 are unknown in the resulting two equations. A simultaneous solution of the two yields $V_B = 0.540$ V and $R_2/R_1 = 5.05$. Note that an additional constraint is needed for resolving the ratio R_2/R_1 into individual values of R_1 and R_2. If not provided by closed-loop performance specifications as in the present case, the designer creates one in accordance with best design principles. It may be related to such concerns as accuracy and precision, power dissipation, footprint, etc.

Next, we determine the specifications of the dc range metrics of the opamp. Since $V_{O(\min)}$ and $V_{O(\max)}$ are already specified for this application, the limits of the opamp output range are to comply with $v_{OL} < 0.150$ V and $v_{OH} > 1.650$ V in accordance with (2.4) and (2.5). As to the limits of the common-mode range, we refer to (2.7) and (2.8) after determining the limits $V_{CM(\min)} = 0.476$ V and $V_{CM(\max)} = 0.723$ V of common-mode swing from (2.11) and (2.6) for two extreme values of v_D.

Finally, we verify the performance of the equivalent circuit of Fig. 2.4(b) with a Spice simulation. This can be done with an operation-point (`.op`) analysis or a dc analysis (`.dc`). In the case of an operation-point analysis, each independent source is assigned a fixed value entered by the user. The simulator determines the dc voltage of each and every node and the dc current of each and every independent voltage source, and prints a table of these variables. The dc analysis differs from the operation-point analysis in that one or two independent sources are swept over a specified range. The corresponding values of node voltages and independent voltage-source currents can be plotted as functions of those sources swept in the dc analysis. In the present example, we must either run two separate operation-point analyses for $V_{D(\min)}$ and $V_{D(\max)}$, or run a single dc analysis sweeping v_D between these two extreme values. We prefer the latter. The Spice schematic of the equivalent circuit of Fig. 2.4(b) is shown in Fig. 2.5. The input file `ex2-1.sp` containing its netlist is as follows:

```
filename: ex2-1.sp          line 1
.param vdd=1.8 vss=0 voh=1.65 vol=0.15 a0=1meg ; line 2
+  vdir=0.25 fgbw=10meg fnd=10g   ; line 2 continuation
.incl opmacro1.sp          ; line 3
x1 1 2 3 opamp             ; line 4
r1 4 2 10k                 ; line 5
r2 2 3 50.5k               ; line 6
vb 4 0 0.54                ; line 7
vd 1 0                     ; line 8
.dc vd 0.476 0.723 1m      ; line 9
.end
```

The second line of the file specifies the parameters of the opamp. As indicated by `vdd=1.8 vss=0`, a single-supply opamp is used. Also note from `voh=1.65` and `vol=0.15` that the output range of the opamp is just as wide as the output swing.

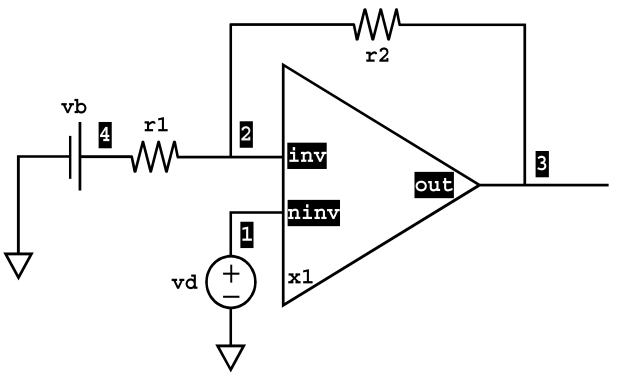

FIGURE 2.5 Simulation schematic of the temperature-sensor equivalent circuit of Example 2.1.

Among the remaining four parameters in line 2, only `a0` is relevant to a first-order dc analysis. This parameter represents the slope of the dc transfer characteristic within the output range. In the ideal opamp assumed throughout the present section this slope should be infinite. The specified `a0=1meg` adequately approximates this assumption. The final two parameters `fgbw` and `fnd` are of no significance in an operation-point analysis or dc analysis. Their values are set arbitrarily.

The third line of the input file includes the opamp macro whose instance is defined in line 4. Lines 5 and 6 define the feedback resistors. We arbitrarily adopt 10-kΩ resistance for R_1. This leads to $R_2 = 50.5$ kΩ since R_2/R_1 has to be 5.05. `vb` and `vd` appearing in lines 7 and 8 define the bias source V_B and diode voltage v_D, respectively.

Also notice the instruction of a dc analysis in line 9. It sweeps `vd` between the expected minimum and maximum levels in 1-mV increments.

For running the simulation, first, change the directory to the folder where `ex2-1.sp` resides. Assuming `c:\spice\chap2` to be the proper folder, enter

```
cd c:\spice\chap2
```

to do that. Next, load the input file by entering

```
ex2-1.sp
```

and start the simulation by entering `run`. Upon completion, entering

```
plot v(3) v(2) v(1)
```

will plot v_O, v_{IN}, and v_{IP}. Notice the virtual equality between v_{IN} and v_{IP}, and verify the limits of the output swing and common-mode swing. ▲

Example 2.2 A closed-loop configuration is qualified as an *inverting* configuration for any input variable that is processed with a negative dc closed-loop gain. If an input variable is processed with a positive dc closed-loop gain, then, the configuration is said to be *noninverting* for that particular input variable. For example, as one can ascertain from (2.13), the configuration shown in Fig. 2.4(b) is inverting for V_B but noninverting for v_D.

Shown in Fig. 2.6 is the most basic noninverting configuration for amplifying a voltage-mode signal source v_i whose source resistance is represented by r_i. V_B is a dc bias-voltage source.

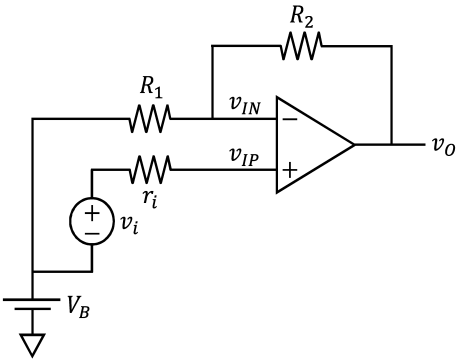

Figure 2.6 The noninverting amplifier of Example 2.2.

1. Derive closed-loop dc gain expressions for v_i and V_B.
2. This amplifier is supposed to provide a closed-loop dc gain $A_{cl,i} = 3$ V/V for v_i whose swing is specified by $V_{i(\min)} = -0.2$ V, $V_{i(\max)} = 0.2$ V. Assuming $V_B = 0.9$ V, determine the output-range and common-mode range specifications of the opamp.

Work We can work out part 1 by (a) recognizing $v_{IP} = V_B + v_i$ from the circuit, (b) assuming $v_{IN} = v_{IP}$ as implied by virtual short, and (c) equating the currents of R_1 and R_2 as

$$\frac{v_{IN} - V_B}{R_1} = \frac{v_O - v_{IN}}{R_2}.$$

Solving these equations for v_O yields the closed-loop dc transfer function

$$v_O = \left(1 + \frac{R_2}{R_1}\right) v_i + V_B, \tag{2.14}$$

which indicates closed-loop dc gains $A_{cl,i} = 1 + (R_2/R_1)$ for v_i and $A_{cl,B} = 1$ for V_B. Incidentally, notice the absence of the source resistance r_i of the signal source in gain expressions. This is due to the fact that the purely capacitive internal loading of the noninverting opamp terminal does not admit any dc current through this resistance. Since source resistances are more inaccurate and more imprecise than those of the resistors used intentionally in the external network, we indeed strive for minimizing their effect on closed-loop gain. Apparently, the noninverting configuration offers a perfect solution in this respect.

We now take the opportunity provided by part 1 of this example to expose the reader to the use of *superposition* in the derivation of a closed-loop gain expression and in the construction of the entire closed-loop transfer function whenever necessary. Superposition, which is applicable to any linear circuit of multiple independent sources, offers a simpler and faster derivation in closed-loop dc analysis. It is applied by disabling all input variables except one, and determining the output variable by analyzing the simplified configuration. This process is repeated for all input variables one by one. Summing up the expressions thus derived for all output variables yields the actual output variable in the presence of all input variables. Recall that an electrical variable is disabled by replacing its source with a zero, that is, short-circuiting a voltage source or open-circuiting a current source. For the closed-loop dc gain due to v_i in Fig. 2.6 for example, disable V_B by replacing it with a short circuit, and write directly $v_{IP} = v_i$, $v_{IN} = v_{IP}$ and $v_{IN}/R_1 = (v_O - v_{IN})/R_2$ from the circuit thus simplified. Solving these equations for v_O/v_i yields $1 + (R_2/R_1)$, which is exactly what we found in the preceding paragraph for $A_{cl,i}$. For determining the gain expression of V_B, first disable v_i by replacing it with a short circuit. Then, write $v_{IP} = V_B$, $v_{IN} = v_{IP}$, and $(v_{IN} - V_B)/R_1 = (v_O - v_{IN})/R_2$ from the circuit thus simplified. Solving these equations for v_O/V_B yields 1, which indeed is what we found in the previous paragraph for $A_{cl,B}$.

In part 2, we first calculate the output swing from (2.14). Using the specified values of $A_{cl,i}$, V_B, and input-signal swing, we obtain $V_{O(\min)} = 0.3$ V and $V_{O(\max)} = 1.5$ V. Output range must satisfy the conditions (2.4) and (2.5) accordingly.

Next, we calculate the limits of the common-mode swing from $v_{CM} = v_{IN} = v_{IP} = V_B + v_i$ as $V_{CM(\min)} = 0.7$ V and $V_{CM(\max)} = 1.1$ V. The common-mode range of the opamp must satisfy (2.7) and (2.8) accordingly.

The reader is now invited to verify the output swing and common-mode swing with a dc simulation. Assume a single-supply ideal opamp of $V_{DD} = 1.8$ V; set V_{OL} and V_{OH} to satisfy the output range determined above; and deploy $r_i = 500\ \Omega$, $R_1 = 10$ kΩ, and $R_2 = 20$ kΩ. ▲

Example 2.3 The *unity-gain buffer* configuration shown in Fig. 2.7 is to be built with an opamp of the following common-mode range and output-range specifications: $V_{IL} = 0.7$ V, $V_{IH} = 2$ V, $V_{OL} = 0.2$ V, $V_{OH} = 1.6$ V. The input signal v_i varies between 0 and 0.5 V. Determine the viable range of bias voltage V_B for this application.

Work Unity-gain buffer is a special case of the noninverting configuration of Fig. 2.6 for $R_2 = 0$ and $R_1 = \infty$. Notice $v_O = v_{IN}$ from the schematic, and $v_{IN} = v_{IP} = V_B + v_i$ due to virtual short. Therefore

$$v_{CM} = v_O = v_i + V_B,$$

which indicates a closed-loop gain of unity for both v_i and V_B. Considering the specified limits of v_i, this equation leads us to

$$V_{CM(\min)} = V_{O(\min)} = V_B,$$

and

$$V_{CM(\max)} = V_{O(\max)} = 0.5\text{V} + V_B.$$

Using these expressions in (2.7) and (2.8) for the common-mode range and in (2.4) and (2.5) for the output range, and considering the specified limits of the two range metrics, we obtain

$$\begin{aligned} V_{IL} = 0.7\,\text{V} &< V_{CM(\min)} = V_B, \\ V_{IH} = 2\,\text{V} &> V_{CM(\max)} = 0.5\text{V} + V_B, \\ V_{OL} = 0.2\,\text{V} &< V_{O(\min)} = V_B, \end{aligned}$$

and

$$V_{OH} = 1.6\,\text{V} > V_{O(\max)} = 0.5\text{V} + V_B.$$

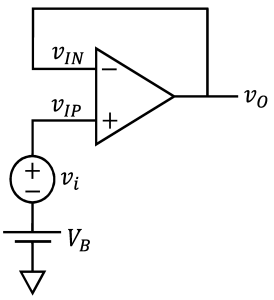

FIGURE 2.7 Unity-gain buffer amplifier of Example 2.3.

Therefore, V_B is constrained by the common-mode range through

$$0.7\,\text{V} < V_B < 1.5\,\text{V},$$

and by the output range through

$$0.2\,\text{V} < V_B < 1.1\,\text{V}.$$

The viable range of V_B satisfying both constraints is therefore described by $0.7\,\text{V} < V_B < 1.1\,\text{V}$.

The reader is now invited to verify the result with dc simulations. Assume a single-supply ideal opamp of $V_{DD} = 1.8\,\text{V}$; set V_{OL} and V_{OH} to their specified values; and, repeat the simulation for different values of V_B inside and outside the viable range determined above. Also verify the unity closed-loop gain. ▲

Example 2.4 Shown in Fig. 2.8 is the most basic inverting configuration for amplifying a voltage-mode signal v_i. r_i represents the source resistance of the signal source. V_B is a dc bias-voltage source.

1. By applying superposition, derive closed-loop dc gain expressions for v_i and V_B and construct the closed-loop dc transfer function.
2. Determine the output-range and common-mode range specifications of the opamp for the following specifications: $R_2 = 10\,\text{k}\Omega$, $R_1 = 2.5\,\text{k}\Omega$, $r_i = 100\,\Omega$, $V_B = 0.9\,\text{V}$, $V_{i(\text{min})} = -0.15\,\text{V}$, $V_{i(\text{max})} = 0.15\,\text{V}$.

Work First, consider the gain for v_i. By shorting out V_B, assuming virtual short, and equating the current of R_2 to that of R_1 and r_i, we obtain

$$\frac{0 - v_i}{R_1 + r_i} = \frac{v_O - 0}{R_2},$$

whose solution for v_O yields the closed-loop gain $-R_2/(R_1 + r_i)$ for v_i. Next, we consider the gain for V_B. By shorting out v_i, assuming virtual short, and equating the current of

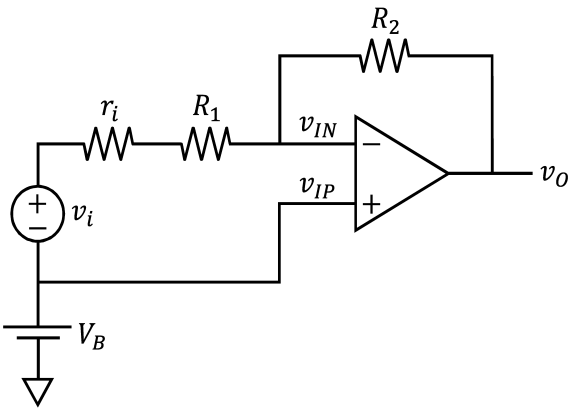

Figure 2.8 Inverting amplifier of Example 2.4.

R_2 to that of R_1 and r_i, we obtain

$$\frac{V_B - V_B}{R_1 + r_i} = \frac{v_O - V_B}{R_2},$$

whose solution for v_O yields the closed-loop gain 1 for V_B. Superposition leads to the following closed-loop dc transfer function:

$$v_O = -\frac{R_2}{R_1 + r_i} v_i + V_B. \tag{2.15}$$

In part 2, we calculate $V_{O(\min)} = 0.323$ V and $V_{O(\max)} = 1.48$ V from (2.15). As usual, output range must comply with (2.4) and (2.5) for these limits of the output swing. Next, notice from the schematic that the common-mode voltage is fixed at $v_{CM} = V_B$ regardless of the value of v_i. Any common-mode range including $V_B = 0.9$ V is therefore good enough for this application.

As a final note, notice the presence of r_i in the closed-loop gain expression for v_i. While a dependence on a source resistance is inevitable in an inverting configuration, we can reduce its effect by selecting large external-network resistances R_1 and R_2.

Simulated verification is again left to the reader as an exercise. ▲

Example 2.5 The transresistance amplifier shown in Fig. 2.9 is to provide a closed-loop gain of $A_{cl,i} = -50$ kΩ for the current-mode signal i_i varying between 0 and 10 μA. V_B is specified as 1 V. Determine the resistance R as well as the common-mode and output ranges.

Work Since $v_{IP} = V_B = 1$ V, virtual short implies $v_{IN} = 1$ V, hence $v_{CM} = 1$ V. Therefore, any common-mode range including 1 V is acceptable for this application. Now equate the signal current to the current flowing in R:

$$i_i = \frac{v_{IN} - v_O}{R}.$$

Since $v_{IN} = V_B$, this expression yields the closed-loop dc transfer function

$$v_O = -Ri_i + V_B, \tag{2.16}$$

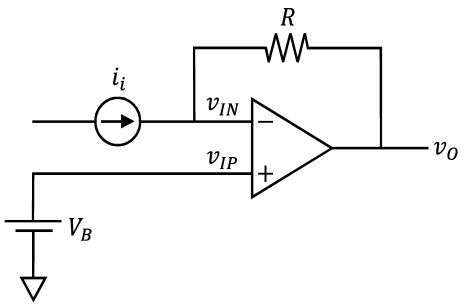

Figure 2.9 Transresistance amplifier of Example 2.5.

which indicates a closed-loop dc gain $A_{cl,i} = -R$ for i_i, and a closed-loop dc gain $A_{cl,B} = 1$ for V_B. The specified value of $A_{cl,i}$ implies $R = 50$ kΩ. Considering also the specified value of V_B and the limits of i_i, (2.16) yields $V_{O(\max)} = 1$ V and $V_{O(\min)} = 0.5$ V. Output range should be wide enough to accommodate these two extremes of the output swing.

The reader will benefit from simulating this application too. Of course, the upstream node of the current source should be tied to ground or any dc voltage-source such as V_B. ▲

2.3 Unified Closed-Loop Model 统一闭环模型

Virtual-short approximation is a very a powerful tool enabling us to analyze the first-order dc response of any closed-loop configuration. Regardless of the complexity of the external network, the analytical procedure is simple, quick, and error-free even for a novice designer. However, this approximation is invalid in the cases of accurate dc response, frequency response, and step response. Modeling of these more sophisticated responses necessitates more complex opamp models, and therefore involves tedious and potentially error-prone circuit analysis. Fortunately, we don't need to face this complexity each time we deal with a specific application because all closed-loop configurations can be represented with one unified closed-loop transfer function for each of these responses. Unification is done by combining a generalized external-network model with a response-specific open-loop transfer function. In this section, we present the generalized external-network model and apply it to the unification of the first-order closed-loop dc transfer function as a simple (and useful) example. Extension to accurate dc response, frequency response, and step response will be presented in Sections 2.4, 2.5, and 2.6, respectively.

2.3.1 A Generalized External-Network Model 通用外部网络模型

Single-ended continuous-time closed-loop configurations deploying linear external-network components can be modeled by the unified block diagram shown in Fig. 2.10(a), where v_O stands for the output voltage and x_j, $j = 1, \ldots, n$, denote the voltage or current sources of input signals or bias. The reader is referred to [1] for the origins of this model. In addition to the opamp, the diagram includes two types of blocks representing the *feedback factor* β and *input factors* α_j, $j = 1, \ldots, n$. All of these factors are defined solely by the external network. β has to be positive in order to establish a negative-feedback loop. α_j may be positive or negative depending on the type of the configuration.

The block diagram shown in Fig. 2.10(a) relates the differential-input voltage v_{ID} of the opamp to x_j and v_O through

$$v_{ID} = \sum_{j=1}^{n} \alpha_j x_j - \beta v_O. \tag{2.17}$$

Since β and α_j are independent of the opamp, this equation is imposed solely by the external network. It represents the generalized external-network model mentioned at the beginning of this section. Independently of (2.17), the opamp itself also relates v_O to v_{ID} through its own open-loop transfer function. By eliminating v_{ID} between the open-loop transfer function and (2.17), we therefore obtain a unified closed-loop transfer function