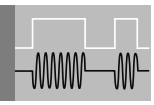
CHAPTER 5



BIPOLAR JUNCTION TRANSISTORS

第5章　双极型晶体管

本章提纲

5.1　双极型晶体管的物理结构
5.2　*npn*型晶体管的传输模型
5.3　*pnp*型晶体管
5.4　传输模型的等效电路
5.5　双极型晶体管的*i*-*v*特性
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5.10　双极型工艺与SPICE模型
5.11　BJT的实际偏置电路
5.12　偏置电路的容差

本章目标

- 理解双极型晶体管的物理结构；
- 理解双极型晶体管的行为及载流子通过基区传输的重要性；
- 理解双极型晶体管及其特性；
- 掌握*npn*晶体管及*pnp*晶体管的区别；
- 理解双极型器件的传输模型；
- 理解BJT的四个工作区；
- 学会每个工作区的简化模型；
- 理解Early效应的来源及模型；
- 了解双极型晶体管的SPICE模型描述；
- 了解偏置电路的最差情况分析及蒙特卡洛（Monte Carlo）分析。

本章导读

本章重点介绍双极型晶体管（BJT）相关概念，包括*npn*晶体管以及*pnp*晶体管，比较全面地讲解了双极型晶体管的物理结构、传输模型、等效电路、输出特性、SPICE模拟以及偏置电路等内容。内容上既有双极型晶体管的发展由来、电路结构，也有相关的模型计算及设计，重点部分以设计实例的形式给出了设计与计算的方法。

双极型晶体管于20世纪40年代末在贝尔电话实验室由Bardeen、Brattain和Shockley发明，并成为第一个商业上成功的三端固态器件，三人也因发明晶体管于1956年获得诺贝尔物理学奖。双极型晶体管的成功面市主要取决于其结构的特点，该晶体管的有源区位于半导体材料表面以下，使得晶体管的工作不受表面特性和清

洁度的制约。因此，最初制作双极型晶体管要比制作MOS管更容易。20世纪50年代后期双极型晶体管开始商业化。20世纪60年代初，出现了第一个集成电路，即电阻-晶体管逻辑门，以及由若干晶体管和电阻构成的运算放大器。

目前，双极型晶体管在分立电路和集成电路设计中仍然广泛使用，特别是在高速、高精度电路中双极型晶体管依然是优先选择的器件，如运算放大器、A/D和D/A转换器以及无线通信产品，锗硅BJT的工作效率在所有硅晶体管中是最高的。

双极型晶体管的物理结构包含三个掺杂半导体区，由*p*型和*n*型交替半导体材料组成的三层夹层构成，可以制作成*npn*或*pnp*两种形式。形成晶体管的发射极将载流子注入基极。大多数载流子横穿基区，并由集电极收集。没有完全穿过基极区域的载流子在基极端子中产生小电流。

本章详细介绍了双极型晶体管的*i-v*特性以及简化传输模型，给出了表征双极型晶体管传输模型的三个独立参数，即饱和电流I_S、正向和反向共发射极电流增益β_F和β_R。β_F非常大，范围是20~500，它表征了BJT的强大的电流放大能力。实际制造中的限制导致双极型晶体管结构具有固有的不对称性，且β_R比β_F小得多，典型值在0~10。

双极型晶体管中，由于每个*pn*结都有正偏和反偏两种状态，因此一共有四种可能的工作区。本章对双极型晶体管的四个工作区进行了定义，并详细介绍了适合于各工作区的简化模型。根据施加到基极-发射极和基极-集电极的偏置电压，决定了晶体管具有的四个工作区，即截止区、正向有源区、反向有源区和饱和区。截止区和饱和区经常用于开关和逻辑电路中。晶体管截止时，等效为断开的开关，当处于饱和区时等效为闭合的开关。正向有源区的双极型晶体管能够提供很高的电压和电流增益，可用于模拟信号的放大。双极型晶体管的*i-v*特性通常以图示的形式表示输出特性和传输特性。输出特性主要表示I_C与V_{CE}的关系，传输特性主要表示I_C与V_{BE}或V_{EB}的关系。

双极型晶体管的特性在许多方面与理想数学模型存在偏差，在晶体管的使用和选择过程中需要考虑许多条件及限制，本章对相关的反向击穿电压、扩散电容、最高频率Early效应（Early effect）等都做了详细的讲解。

为了得到双极型晶体管的综合仿真模型，除了运用晶体管的物理结构相关知识外，还需要晶体管传输模型表达式并进行相关实验。本章在分析双极型晶体管工艺的基础上给出了双极型晶体管的SPICE模型及其简化，给出了SPICE表达式中常用的参数。理解SPICE内部模型，有助于判断与分析SPICE仿真结果与仿真器件的特定应用是否一致。

双极型晶体管的偏置电路设计与分析是研究双极型晶体管的重要内容。本章研究了双极型晶体管的实际偏置电路，对四电阻网络的设计做了深入研究。偏置的目标是建立已知的静态工作点或Q点，表示晶体管最初所处的工作区。对于双极型晶体管而言，*npn*晶体管的Q点由集电极电流的直流量I_C和集电极-发射极电压V_{CE}表示；*pnp*晶体管的Q点则由集电极电流的直流量I_C和发射极-集电极电压V_{EC}表示。四电阻偏置电路可以很好地控制Q点，是能够保持晶体管Q点稳定的最好的电路之一。

本章详细讲解了四电阻偏置的电路、设计目标，提供了用于偏置双极型晶体管的四电阻偏置电路和二电阻偏置电路实例，并给出了四电阻偏置电路设计中的迭代分析方法。

无论电路是在实验室制作还是批量的集成电路制造，电路元件都存在参数取值的容差。分立电阻容差可以为10%、5%或者1%，而集成电路中电阻的容差会更大（±30%）。电源电压的容差一般为5%~10%。电路元件的容差会对偏置电路设计和分析产生很大的影响，本章重点给出了两种分析元件容差对电路影响的方法，即最差情况分析和统计蒙特卡洛分析，并给出了分析实例。在最差情况分析中，将元件的参数值取极限值，得到的结果往往很差。蒙特卡洛方法分析了大量随机选择的电路，以建立电路性能统计分布的实际估计。计算机高级语言、电子表格或者MATLAB中的随机数据发生器可以为蒙特卡洛分析提供随机的元件数值。SPICE中的一些电路分析软件包还提供蒙特卡洛分析选项。

Chapter Outline

Chapter Goals

- Explore the physical structure of the bipolar transistor
- Understand bipolar transistor action and the importance of carrier transport across the base region
- Study the terminal characteristics of the BJT
- Explore the differences between *npn* and *pnp* transistors
- Develop the transport model for the bipolar device
- Define the four regions of operation of the BJT
- Explore model simplifications for each region of operation
- Understand the origin and modeling of the Early effect
- Present the SPICE model for the bipolar transistor
- Provide examples of worst-case and Monte Carlo analysis of bias circuits

November 2017 is the 70th anniversary of the discovery of the bipolar transistor by John Bardeen and Walter Brattain at Bell Laboratories. In a matter of a few months, William Shockley managed to develop a theory describing the operation of the bipolar junction transistor. Only a few years later in 1956, Bardeen, Brattain, and Shockley received the Nobel Prize in Physics for the discovery of the transistor.

John Bardeen, William Shockley, and Walter Brattain in Brattain's Laboratory in 1948.
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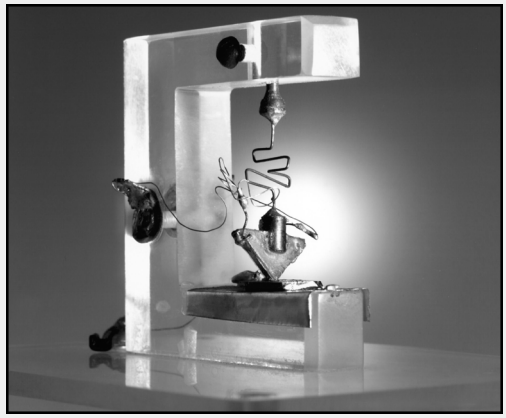

The first germanium bipolar transistor
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In June 1948, Bell Laboratories held a major press conference to announce the discovery (which of course went essentially unnoticed by the public). Later in 1952, Bell Laboratories, operating under legal consent decrees, made licenses for the transistor available for the modest fee of $25,000 plus future royalty payments. About this time, Gordon Teal, another member of the solid-state group, left Bell Laboratories to work on the transistor at Geophysical Services Inc., which subsequently became Texas Instruments (TI). There he made the first silicon transistors, and

TI marketed the first all transistor radio. Another of the early licensees of the transistor was Tokyo Tsushin Kogyo which became the Sony Company in 1955. Sony subsequently sold a transistor radio with a marketing strategy based upon the idea that everyone could now have their own personal radio; thus was launched the consumer market for transistors. A very interesting account of these and other developments can be found in [1, 2] and their references.

Following its invention and demonstration in the late 1940s by Bardeen, Brattain, and Shockley at Bell Laboratories, the **bipolar junction transistor,** or **BJT,** became the first commercially successful three-terminal solid-state device. Its commercial success was based on its structure in which the active base region of the transistor is below the surface of the semiconductor material, making it much less dependent on surface properties and cleanliness. Thus, it was initially easier to manufacture BJTs than MOS transistors, and commercial bipolar transistors were available in the late 1950s. The first integrated circuits, resistor-transistor logic gates and operational amplifiers, consisting of a few transistors and resistors appeared in the early 1960s.

While the FET has become the dominant device technology in modern integrated circuits, bipolar transistors are still widely used in both discrete and integrated circuit design. In particular, the BJT is still the preferred device in many applications that require high speed and/or high precision. Typical of these application areas are circuits for the growing families of wireless computing and communication products, and silicon-germanium (SiGe) BJTs offer the highest operating frequencies of any silicon transistor.

The bipolar transistor is composed of a sandwich of three doped semiconductor regions and comes in two forms: the *npn* transistor and the *pnp* transistor. Performance of the bipolar transistor is dominated by *minority-carrier* transport via diffusion and drift in the central region of the transistor. Because carrier mobility and diffusivity are higher for electrons than holes, the *npn* transistor is an inherently higher-performance device than the *pnp* transistor. In Part III of this book, we will learn that the bipolar transistor typically offers a much higher voltage gain capability than the FET. On the other hand, the BJT input resistance is much lower, because a current must be supplied to the control electrode.

Our study of the BJT begins with a discussion of the *npn* transistor, followed by a discussion of the *pnp* device. The **transport model,** a simplified version of the Gummel-Poon model, is developed and used as our mathematical model for the behavior of the BJT. Four regions of operation of the BJT are defined and simplified models developed for each region. Examples of circuits that can be used to bias the bipolar transistor are presented. The chapter closes with a discussion of the worst-case and Monte Carlo analyses of the effects of tolerances on bias circuits.

5.1 PHYSICAL STRUCTURE OF THE BIPOLAR TRANSISTOR

The bipolar transistor structure consists of three alternating layers of *n*- and *p*-type semiconductor material. These layers are referred to as the **emitter (E), base (B),** and **collector (C)**. Either an ***npn*** or a ***pnp*** **transistor** can be fabricated. The behavior of the device can be seen from the simplified cross section of the *npn* transistor in Fig. 5.1(a). During normal operation, a majority of the current enters the collector terminal, crosses the base region, and exits from the emitter terminal. A small current also enters the base terminal, crosses the base-emitter junction of the transistor, and exits the emitter.

The most important part of the bipolar transistor is the active base region between the dashed lines directly beneath the heavily doped ($n+$) emitter. Carrier transport in this region dominates the i-v characteristics of the BJT. Figure 5.1(b) illustrates the rather complex physical structure actually used to realize an *npn* transistor in integrated circuit form. Most of the structure in Fig. 5.1(b) is required to fabricate the external contacts to the collector, base, and emitter regions and to isolate one bipolar transistor from another. In the *npn* structure shown, collector current i_C and base current i_B enter the

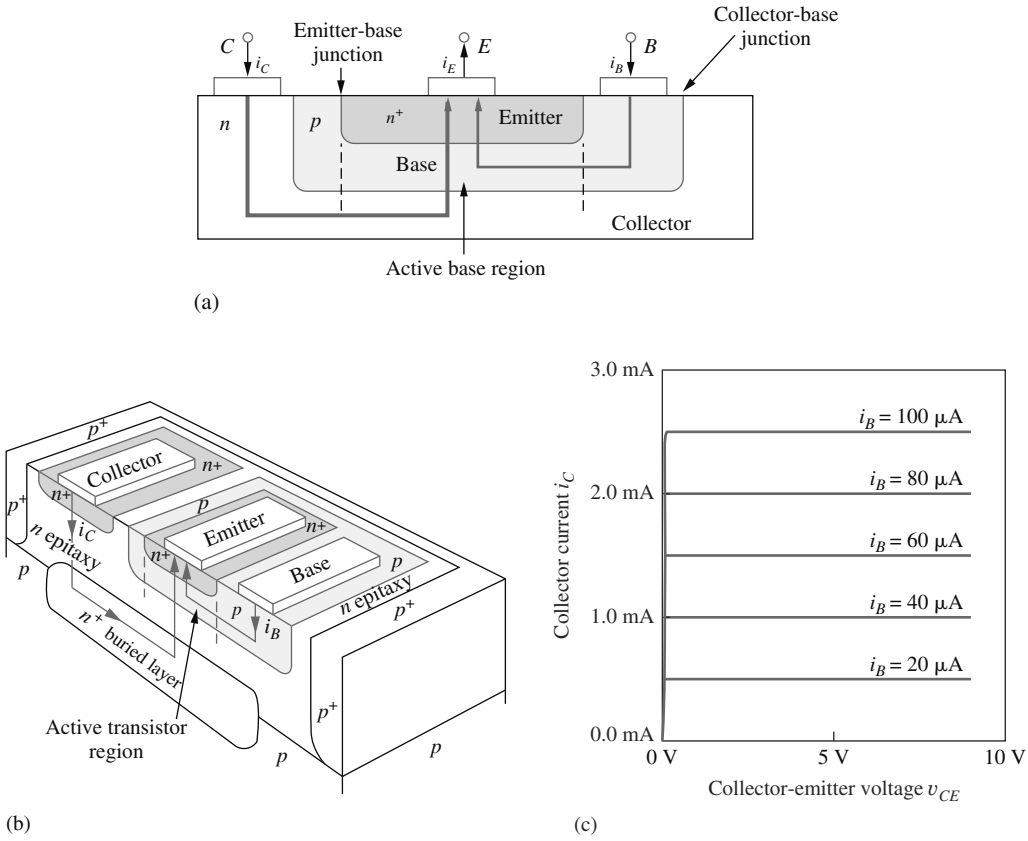


Figure 5.1 (a) Simplified cross section of an *npn* transistor with currents that occur during "normal" operation; (b) three-dimensional view of an integrated *npn* bipolar junction transistor; (c) output characteristics of an *npn* transistor.

collector (C) and base (B) terminals of the transistor, and emitter current i_E exits from the emitter (E) terminal. An example of the **output characteristics** of the bipolar transistor appears in Fig. 5.1(c), which plots collector current i_C versus collector-emitter voltage v_{CE} with base current as a parameter. The characteristics exhibit an appearance very similar to the output characteristics of the field-effect transistor. We find that a primary difference, however, is that a significant dc current must be supplied to the base of the device, whereas the dc gate current of the FET is zero. In the sections that follow, a mathematical model is developed for these i-v characteristics for both *npn* and *pnp* transistors.

5.2 THE TRANSPORT MODEL FOR THE *npn* TRANSISTOR

Figure 5.2 represents a conceptual model for the active region of the *npn* bipolar junction transistor structure. At first glance, the BJT appears to simply be two *pn* junctions connected back to back. However, the central region (the base) is very thin (0.1 to 100 μm), and the close proximity of the two junctions leads to coupling between the two diodes. This coupling is the essence of the bipolar device. The lower *n*-type region (the emitter) injects electrons into the *p*-type base region of the device. Almost all these injected electrons travel across the narrow base region and are removed (or collected) by the upper *n*-type region (the collector).

The three terminal currents are the **collector current i_C**, the **emitter current i_E**, and the **base current i_B.** The base-emitter voltage v_{BE} and the base-collector voltage v_{BC} applied to the two *pn* junctions in Fig. 5.2 determine the magnitude of these three currents in the bipolar transistor and

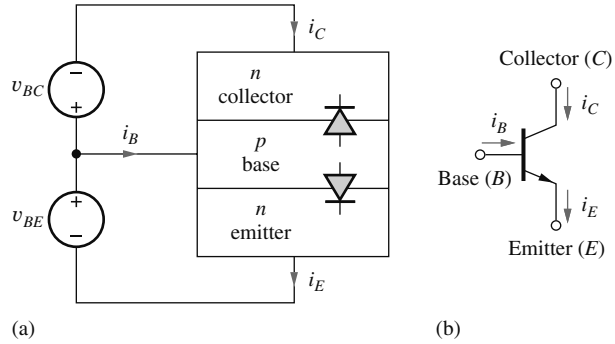


Figure 5.2 (a) Idealized *npn* transistor structure for a general-bias condition; (b) circuit symbol for the *npn* transistor.

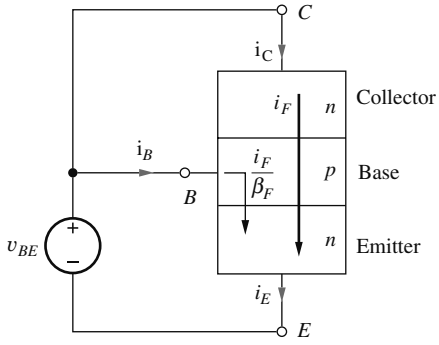


Figure 5.3 *npn* transistor with v_{BE} applied and $v_{BC} = 0$.

TABLE 5.1
Common-Emitter and Common-Base Current Gain Comparison

α_F or α_R	$\beta_F = \frac{\alpha_F}{1-\alpha_F}$ or $\beta_R = \frac{\alpha_R}{1-\alpha_R}$
0.1	0.11
0.5	1
0.9	9
0.95	19
0.99	99
0.998	499

are defined as positive when they forward-bias their respective *pn* junctions. The arrows indicate the directions of positive current in most *npn* circuit applications. The circuit symbol for the *npn* transistor appears in Fig. 5.2(b). The arrow part of the symbol identifies the emitter terminal and indicates that dc current normally exits the emitter of the *npn* transistor.

5.2.1 FORWARD CHARACTERISTICS

To facilitate both hand and computer analysis, we need to construct a mathematical model that closely matches the behavior of the transistor, and equations that describe the static *i-v* characteristics of the device can be constructed by summing currents within the transistor structure.[1] In Fig. 5.3, an arbitrary voltage v_{BE} is applied to the base-emitter junction, and the voltage applied to the base-collector junction is set to zero. The base-emitter voltage establishes emitter current i_E, which equals the total current crossing the base-emitter junction. This current is composed of two components. The largest portion, the **forward-transport current i_F,** enters the collector, travels completely across the very narrow base region, and exits the emitter terminal. The collector current i_C is equal to i_F, which has the form of an ideal diode current

$$i_C = i_F = I_S \left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right] \tag{5.1}$$

[1] The differential equations that describe the internal physics of the BJT are linear second-order differential equations. These equations are linear in terms of the hole and electron concentrations; the currents are directly related to these carrier concentrations. Thus, superposition can be used with respect to the currents flowing in the device.

Parameter $\boldsymbol{I_S}$ is the **transistor saturation current**—that is, the saturation current of the bipolar transistor. I_S is proportional to the cross-sectional area of the active base region of the transistor, and can have a wide range of values:

$$10^{-18}\ \text{A} \leq I_S \leq 10^{-9}\ \text{A}$$

In Eq. (5.1), V_T should be recognized as the thermal voltage introduced in Chapter 2 and given by $V_T = kT/q \cong 0.025$ V at room temperature.

In addition to i_F, a second, much smaller component of current crosses the base-emitter junction. This current forms the base current i_B of the transistor, and it is directly proportional to i_F:

$$i_B = \frac{i_F}{\beta_F} = \frac{I_S}{\beta_F}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \tag{5.2}$$

Parameter $\boldsymbol{\beta_F}$ is called the **forward** (or **normal**[2]) **common-emitter current gain.** Its value typically falls in the range

$$10 \leq \beta_F \leq 500$$

Emitter current i_E can be calculated by treating the transistor as a super node for which

$$i_C + i_B = i_E \tag{5.3}$$

Adding Eqs. (5.1) and (5.2) together yields

$$i_E = \left(I_S + \frac{I_S}{\beta_F}\right)\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \tag{5.4}$$

which can be rewritten as

$$i_E = I_S\left(\frac{\beta_F + 1}{\beta_F}\right)\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] = \frac{I_S}{\alpha_F}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \tag{5.5}$$

The parameter $\boldsymbol{\alpha_F}$ is called the **forward** (or **normal**[3]) **common-base current gain,** and its value typically falls in the range

$$0.95 \leq \alpha_F < 1.0$$

The parameters α_F and β_F are related by

$$\alpha_F = \frac{\beta_F}{\beta_F + 1} \qquad \text{or} \qquad \beta_F = \frac{\alpha_F}{1 - \alpha_F} \tag{5.6}$$

Equations (5.1), (5.2), and (5.5) express the fundamental physics-based characteristics of the bipolar transistor. The three terminal currents are all exponentially dependent on the base-emitter voltage of the transistor. This is a much stronger nonlinear dependence than the square-law behavior of the FET.

For the bias conditions in Fig. 5.3, the transistor is actually operating in a region of high current gain, called the **forward-active region**[4] of operation, which is discussed more fully in Sec. 5.9. Three extremely useful auxiliary relationships are valid in the forward-active region. The first two

[2] β_N is sometimes used to represent the normal common-emitter current gain.

[3] α_N is sometimes used to represent the normal common-base current gain.

[4] Four regions of operation are fully defined in Sec. 5.6.

can be found from the ratio of the collector and base current in Eqs. (5.1) and (5.2):

$$\frac{i_C}{i_B} = \beta_F \qquad \text{or} \qquad i_C = \beta_F i_B \qquad \text{and} \qquad i_E = (\beta_F + 1) i_B \tag{5.7}$$

using Eq. (5.3). The third relationship is found from the ratio of the collector and emitter currents in Eqs. (5.1) and (5.5):

$$\frac{i_C}{i_E} = \alpha_F \qquad \text{or} \qquad i_C = \alpha_F i_E \tag{5.8}$$

Equation (5.7) expresses important and useful properties of the bipolar transistor: The transistor "amplifies" (magnifies) its base current by the factor β_F. Because the current gain $\beta_F \gg 1$, injection of a small current into the base of the transistor produces a much larger current in both the collector and the emitter terminals. Equation (5.8) indicates that the collector and emitter currents are almost identical because $\alpha_F \cong 1$.

5.2.2 REVERSE CHARACTERISTICS

Now consider the transistor in Fig. 5.4, in which voltage v_{BC} is applied to the base-collector junction, and the base-emitter junction is zero-biased. The base-collector voltage establishes the collector current i_C, now crossing the base-collector junction. The largest portion of the collector current, the reverse-transport current i_R, enters the emitter, travels completely across the narrow base region, and exits the collector terminal. Current i_R has a form identical to i_F:

$$i_R = I_S \left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1 \right] \qquad \text{and} \qquad i_E = -i_R \tag{5.9}$$

except the controlling voltage is now v_{BC}.

In this case, a fraction of the current i_R must also be supplied as base current through the base terminal:

$$i_B = \frac{i_R}{\beta_R} = \frac{I_S}{\beta_R} \left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1 \right] \tag{5.10}$$

Parameter $\boldsymbol{\beta_R}$ is called the **reverse** (or **inverse**[5]) **common-emitter current gain.**

In Chapter 4, we discovered that the FET was an inherently symmetric device. For the bipolar transistor, Eqs. (5.1) and (5.9) show the symmetry that is inherent in the current that traverses the base region of the bipolar transistor. However, the impurity doping levels of the emitter and collector regions of the BJT structure are quite asymmetric, and this fact causes the base currents in the

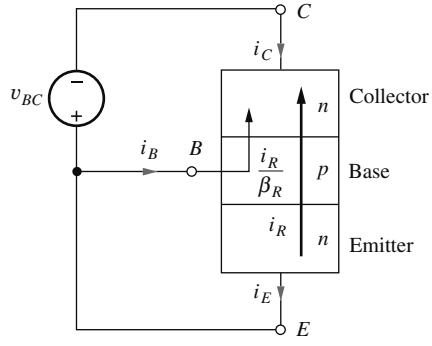


Figure 5.4 Transistor with v_{BC} applied and $v_{BE} = 0$.

[5] β_I is sometimes used to represent the inverse common-emitter current gain.

forward and reverse modes to be significantly different. For typical BJTs, $0 < \beta_R \leq 10$ whereas $10 \leq \beta_F \leq 500$.

The collector current in Fig. 5.4 can be found by combining the base and emitter currents, as was done to obtain Eq. (5.5):

$$i_C = -\frac{I_S}{\alpha_R}\left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1\right] \tag{5.11}$$

in which the parameter $\boldsymbol{\alpha_R}$ is called the **reverse** (or **inverse**[6]) **common-base current gain:**

$$\alpha_R = \frac{\beta_R}{\beta_R + 1} \qquad \text{or} \qquad \beta_R = \frac{\alpha_R}{1 - \alpha_R} \tag{5.12}$$

Typical values of α_R fall in the range

$$0 < \alpha_R \leq 0.95$$

Values of the common-base current gain α and the common-emitter current gain β are compared in Table 5.1 on page 218. Because α_F is typically greater than 0.95, β_F can be quite large. Values ranging from 10 to 500 are quite common for β_F, although it is possible to fabricate special-purpose transistors[7] with β_F as high as 5000. In contrast, α_R is typically less than 0.5, which results in values of β_R of less than 1.

EXERCISE: **(a) What values of β correspond to $\alpha = 0.970, 0.993, 0.250$? (b) What values of α correspond to $\beta = 40, 200, 3$?**

ANSWERS: **(a) 32.3; 142; 0.333 (b) 0.976; 0.995; 0.750**

5.2.3 THE COMPLETE TRANSPORT MODEL EQUATIONS FOR ARBITRARY BIAS CONDITIONS

Combining the expressions for the two collector, emitter, and base currents from Eqs. (5.1) and (5.11), (5.4) and (5.9), and (5.2) and (5.10) yields expressions for the total collector, emitter, and base currents for the *npn* transistor that are valid for the completely general-bias voltage situation in Fig. 5.2:

$$\begin{aligned}
i_C &= I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right) - \exp\left(\frac{v_{BC}}{V_T}\right)\right] - \frac{I_S}{\beta_R}\left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1\right] \\
i_E &= I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right) - \exp\left(\frac{v_{BC}}{V_T}\right)\right] + \frac{I_S}{\beta_F}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \\
i_B &= \frac{I_S}{\beta_F}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] + \frac{I_S}{\beta_R}\left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1\right]
\end{aligned} \tag{5.13}$$

From this equation set, we see that three parameters are required to characterize an individual BJT: I_S, β_F, and β_R. (Remember that temperature is also an important parameter because $V_T = kT/q$.)

The first term in both the emitter and collector current expressions in Eqs. (5.13) is

$$i_T = I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right) - \exp\left(\frac{v_{BC}}{V_T}\right)\right] \tag{5.14}$$

which represents the current being transported completely across the base region of the transistor. Equation (5.14) demonstrates the symmetry that exists between the base-emitter and base-collector voltages in establishing the dominant current in the bipolar transistor.

[6] α_I is sometimes used to represent the inverse common-base current gain.

[7] These devices are often called "super-beta" transistors.

Equation (5.13) actually represents a simplified version of the more complex **Gummel-Poon model** [3, 4] and form the heart of the BJT model used in the SPICE simulation program. The full Gummel-Poon model accurately describes the characteristics of BJTs over a wide range of operating conditions, and it has largely supplanted its predecessor, the **Ebers-Moll model** [5] (see Prob. 5.23).

EXAMPLE 5.1 TRANSPORT MODEL CALCULATIONS

The advantage of the full transport model is that it can be used to estimate the currents in the bipolar transistor for any given set of bias voltages.

PROBLEM Use the transport model equations to find the terminal voltages and currents in the circuit in Fig. 5.5 in which an *npn* transistor is biased by two dc voltage sources.

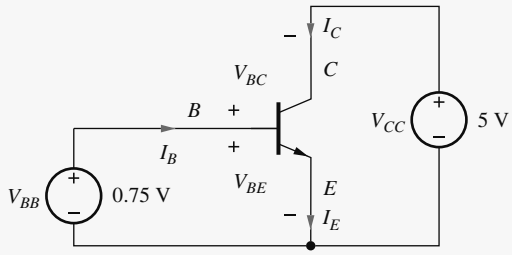


Figure 5.5 *npn* transistor circuit example: $I_S = 10^{-16}$ A, $\beta_F = 50$, $\beta_R = 1$.

SOLUTION **Known Information and Given Data:** The *npn* transistor in Fig. 5.5 is biased by two dc sources $V_{BB} = 0.75$ V and $V_{CC} = 5.0$ V. The transistor parameters are $I_S = 10^{-16}$ A, $\beta_F = 50$, and $\beta_R = 1$.

Unknowns: Junction bias voltages V_{BE} and V_{BC}; emitter current I_E, collector current I_C, base current I_B

Approach: Determine V_{BE} and V_{BC} from the circuit. Use these voltages and the transistor parameters to calculate the currents using Eq. (5.13).

Assumptions: The transistor is modeled by the transport equations and is operating at room temperature with $V_T = 25.0$ mV.

Analysis: In this circuit, the base emitter voltage V_{BE} is set directly by source V_{BB}, and the base collector voltage is the difference between V_{BB} and V_{CC}:

$$V_{BE} = V_{BB} = 0.75 \text{ V}$$
$$V_{BC} = V_{BB} - V_{CC} = 0.75 \text{ V} - 5.00 \text{ V} = -4.25 \text{ V}$$

Substituting these voltages into Eqs. (5.13) along with the transistor parameters yields

$$I_C = 10^{-16} \text{ A} \left[\exp\left(\frac{0.75 \text{ V}}{0.025 \text{ V}}\right) - \cancelto{0}{\exp\left(\frac{-4.75 \text{ V}}{0.025 \text{ V}}\right)} \right] - \frac{10^{-16}}{1} \text{ A} \left[\cancelto{0}{\exp\left(\frac{-4.75 \text{ V}}{0.025 \text{ V}}\right)} - 1 \right]$$

$$I_E = 10^{-16} \text{ A} \left[\exp\left(\frac{0.75 \text{ V}}{0.025 \text{ V}}\right) - \cancelto{0}{\exp\left(\frac{-4.75 \text{ V}}{0.025 \text{ V}}\right)} \right] + \frac{10^{-16}}{50} \text{ A} \left[\exp\left(\frac{0.75 \text{ V}}{0.025 \text{ V}}\right) - 1 \right]$$

$$I_B = \frac{10^{-16}}{50} \text{ A} \left[\exp\left(\frac{0.75 \text{ V}}{0.025 \text{ V}}\right) - 1 \right] + \frac{10^{-16}}{1} \text{ A} \left[\cancelto{0}{\exp\left(\frac{-4.75 \text{ V}}{0.025 \text{ V}}\right)} - 1 \right]$$

and evaluating these expressions gives

$$I_C = 1.07 \text{ mA} \qquad I_E = 1.09 \text{ mA} \qquad I_B = 21.4 \ \mu\text{A}$$

Check of Results: The sum of the collector and base currents equals the emitter current as required by KCL for the transistor treated as a super node. Also, the terminal currents range from microamperes to milliamperes, which are reasonable for most transistors.

Discussion: Note that the collector-base junction in Fig. 5.5 is reverse-biased, so the terms containing V_{BC} become negligibly small. In this example, the transistor is biased in the forward-active region of operation for which

$$\beta_F = \frac{I_C}{I_B} = \frac{1.07 \text{ mA}}{0.0214 \text{ mA}} = 50 \qquad \text{and} \qquad \alpha_F = \frac{I_C}{I_E} = \frac{1.07 \text{ mA}}{1.09 \text{ mA}} = 0.982$$

EXERCISE: Repeat the example problem for $I_S = 10^{-15}$ A, $\beta_F = 100$, $\beta_R = 0.50$, $V_{BE} = 0.70$ V, and $V_{CC} = 10$ V.

ANSWERS: $I_C = 1.45$ mA, $I_E = 1.46$ mA, and $I_B = 14.5 \ \mu$A

In Secs. 5.5 to 5.11 we completely define four different regions of operation of the transistor and find simplified models for each region. First, however, let us develop the transport model for the *pnp* transistor in a manner similar to that for the *npn* transistor.

5.3 THE *pnp* TRANSISTOR

In Chapter 4, we found we could make either NMOS or PMOS transistors by simply interchanging the *n*- and *p*-type regions in the device structure. One might expect the same to be true of bipolar transistors, and we can indeed fabricate *pnp* transistors as well as *npn* transistors.

The *pnp* transistor is fabricated by reversing the layers of the transistor, as diagrammed in Fig. 5.6. The transistor has been drawn with the emitter at the top of the diagram, as it appears in most circuit diagrams throughout this book. The arrows again indicate the normal directions of positive current in the *pnp* transistor in most circuit applications. The voltages applied to the two *pn* junctions are the emitter-base voltage v_{EB} and the collector-base voltage v_{CB}. These voltages are again positive when they forward-bias their respective *pn* junctions. Collector current i_C and base current i_B exit the transistor terminals, and the emitter current i_E enters the device. The circuit symbol for the *pnp*

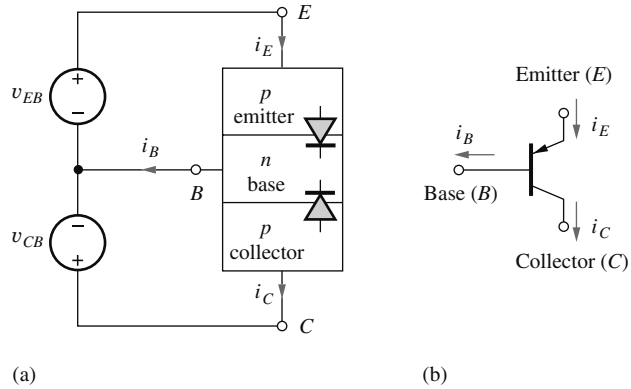


Figure 5.6 (a) Idealized *pnp* transistor structure for a general-bias condition; (b) circuit symbol for the *pnp* transistor.

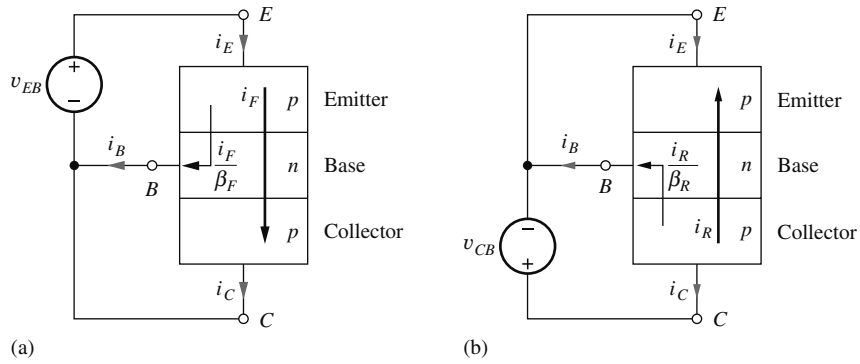


Figure 5.7 (a) *pnp* transistor with v_{EB} applied and $v_{CB} = 0$; (b) *pnp* transistor with v_{CB} applied and $v_{EB} = 0$.

transistor appears in Fig. 5.6(b). The arrow identifies the emitter of the *pnp* transistor and points in the direction of normal positive-emitter current.

Equations that describe the static *i-v* characteristics of the *pnp* transistor can be constructed by summing currents within the structure just as for the *npn* transistor. In Fig. 5.7(a), voltage v_{EB} is applied to the emitter-base junction, and the collector-base voltage is set to zero. The emitter-base voltage establishes forward-transport current i_F that traverses the narrow base region and base current i_B that crosses the emitter-base junction of the transistor:

$$i_C = i_F = I_S\left[\exp\left(\frac{v_{EB}}{V_T}\right) - 1\right] \qquad i_B = \frac{i_F}{\beta_F} = \frac{I_S}{\beta_F}\left[\exp\left(\frac{v_{EB}}{V_T}\right) - 1\right]$$

and (5.15)

$$i_E = i_C + i_B = I_S\left(1 + \frac{1}{\beta_F}\right)\left[\exp\left(\frac{v_{EB}}{V_T}\right) - 1\right]$$

In Fig. 5.7(b), a voltage v_{CB} is applied to the collector-base junction, and the emitter-base junction is zero-biased. The collector-base voltage establishes the reverse-transport current i_R and base current i_B:

$$-i_E = i_R = I_S\left[\exp\left(\frac{v_{CB}}{V_T}\right) - 1\right] \qquad i_B = \frac{i_R}{\beta_R} = \frac{I_S}{\beta_R}\left[\exp\left(\frac{v_{CB}}{V_T}\right) - 1\right]$$

and (5.16)

$$i_C = -I_S\left(1 + \frac{1}{\beta_R}\right)\left[\exp\left(\frac{v_{CB}}{V_T}\right) - 1\right]$$

where the collector current is given by $i_C = i_E - i_B$.

For the general-bias voltage situation in Fig. 5.6, Eqs. (5.15) and (5.16) are combined to give the total collector, emitter, and base currents of the *pnp* transistor:

$$\begin{aligned} i_C &= I_S\left[\exp\left(\frac{v_{EB}}{V_T}\right) - \exp\left(\frac{v_{CB}}{V_T}\right)\right] - \frac{I_S}{\beta_R}\left[\exp\left(\frac{v_{CB}}{V_T}\right) - 1\right] \\ i_E &= I_S\left[\exp\left(\frac{v_{EB}}{V_T}\right) - \exp\left(\frac{v_{CB}}{V_T}\right)\right] + \frac{I_S}{\beta_F}\left[\exp\left(\frac{v_{EB}}{V_T}\right) - 1\right] \\ i_B &= \frac{I_S}{\beta_F}\left[\exp\left(\frac{v_{EB}}{V_T}\right) - 1\right] + \frac{I_S}{\beta_R}\left[\exp\left(\frac{v_{CB}}{V_T}\right) - 1\right] \end{aligned} \qquad (5.17)$$

These equations represent the simplified Gummel-Poon or transport model equations for the *pnp* transistor and can be used to relate the terminal voltages and currents of the *pnp* transistor for any general-bias condition. Note that these equations are identical to those for the *npn* transistor except that v_{EB} and v_{CB} replace v_{BE} and v_{BC}, respectively, and are a result of our careful choice for the direction of positive currents in Figs. 5.2 and 5.6.

EXERCISE: Find I_C, I_E, and I_B for a *pnp* transistor if $I_S = 10^{-16}$ A, $\beta_F = 75$, $\beta_R = 0.40$, $V_{EB} = 0.75$ V, and $V_{CB} = +0.70$ V.

ANSWERS: $I_C = 0.563$ mA, $I_E = 0.938$ mA, $I_B = 0.376$ mA

5.4 EQUIVALENT CIRCUIT REPRESENTATIONS FOR THE TRANSPORT MODELS

For circuit simulation, as well as hand analysis purposes, the transport model equations for the *npn* and *pnp* transistors can be represented by the equivalent circuits shown in Fig. 5.8(a) and (b), respectively. In the *npn* model in Fig. 5.8(a), the total transport current i_T traversing the base is determined by I_S, v_{BE}, and v_{BC}, and is modeled by the current source i_T:

$$i_T = i_F - i_R = I_S \left[\exp\left(\frac{v_{BE}}{V_T}\right) - \exp\left(\frac{v_{BC}}{V_T}\right) \right] \tag{5.18}$$

The diode currents correspond directly to the two components of the base current:

$$i_B = \frac{I_S}{\beta_F} \left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right] + \frac{I_S}{\beta_R} \left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1 \right] \tag{5.19}$$

Directly analogous arguments hold for the circuit elements in the *pnp* circuit model of Fig. 5.8(b).

EXERCISE: Find I_T if $I_S = 10^{-15}$ A, $V_{BE} = 0.75$ V, and $V_{BC} = -2.0$ V.

ANSWER: 10.7 mA

EXERCISE: Find the dc transport current I_T for the transistor in Example 5.1 on page 222.

ANSWER: $I_T = 1.07$ mA

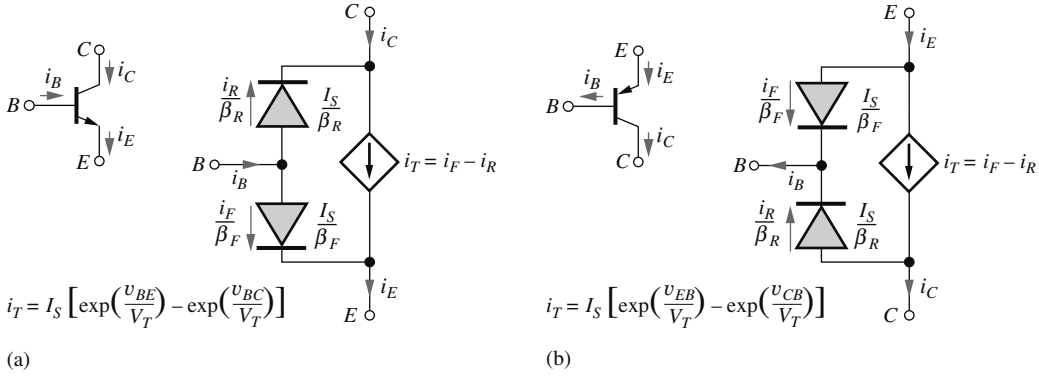


Figure 5.8 (a) Transport model equivalent circuit for the *npn* transistor; (b) transport model equivalent circuit for the *pnp* transistor.

5.5 THE *i-v* CHARACTERISTICS OF THE BIPOLAR TRANSISTOR

Two complementary views of the *i-v* behavior of the BJT are represented by the device's **output characteristic** and **transfer characteristic.** (Remember that similar characteristics were presented for the FETs in Chapter 4.) The output characteristics represent the relationship between the collector current and collector-emitter or collector-base voltage of the transistor, whereas the transfer characteristic relates the collector current to the base-emitter voltage. A knowledge of both *i-v* characteristics is basic to understanding the overall behavior of the bipolar transistor.

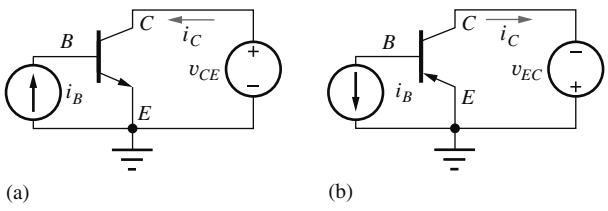
5.5.1 OUTPUT CHARACTERISTICS

Circuits for measuring or simulating the **common-emitter output characteristics** are shown in Fig. 5.9. In these circuits, the base of the transistor is driven by a constant current source, and the output characteristics represent a graph of i_C vs. v_{CE} for the *npn* transistor (or i_C vs. v_{EC} for the *pnp*) with base current i_B as a parameter. Note that the Q-point (I_C, V_{CE}) or (I_C, V_{EC}) locates the BJT operating point on the output characteristics.

First, consider the *npn* transistor operating with $v_{CE} \geq 0$, represented by the first quadrant of the graph in Fig. 5.10. For $i_B = 0$, the transistor is nonconducting or cut off. As i_B increases above 0, i_C also increases. For $v_{CE} \geq v_{BE}$, the *npn* transistor is in the forward-active region, and collector current is independent of v_{CE} and equal to $\beta_F i_B$. Remember, it was demonstrated earlier that $i_C \cong \beta_F i_B$ in the forward-active region. For $v_{CE} \leq v_{BE}$, the transistor enters the **saturation region** of operation in which the total voltage between the collector and emitter terminals of the transistor is small.

It is important to note that the saturation region of the BJT does not correspond to the saturation region of the FET. The forward-active region (or just **active region**) of the BJT corresponds to the saturation region of the FET. When we begin our discussion of amplifiers in Part III, we will simply apply the term active region to both devices. The active region is the region most often used in transistor implementations of amplifiers.

In the third quadrant for $v_{CE} \leq 0$, the roles of the collector and emitter reverse. For $v_{BE} \leq v_{CE} \leq 0$, the transistor remains in saturation. For $v_{CE} \leq v_{BE}$, the transistor enters the **reverse-active region**, in which the *i-v* characteristics again become independent of v_{CE}, and now $i_C \cong -(\beta_R + 1)i_B$. The reverse-active region curves have been plotted for a relatively large value of reverse



(a) (b)

Figure 5.9 Circuits for determining common-emitter output characteristics: (a) *npn* transistor, (b) *pnp* transistor.

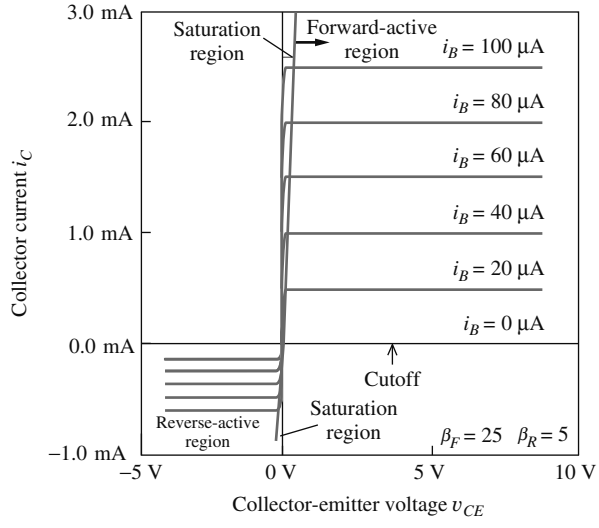


Figure 5.10 Common-emitter output characteristics for the bipolar transistor (i_C vs. v_{CE} for the *npn* transistor or i_C vs. v_{EC} for the *pnp* transistor).

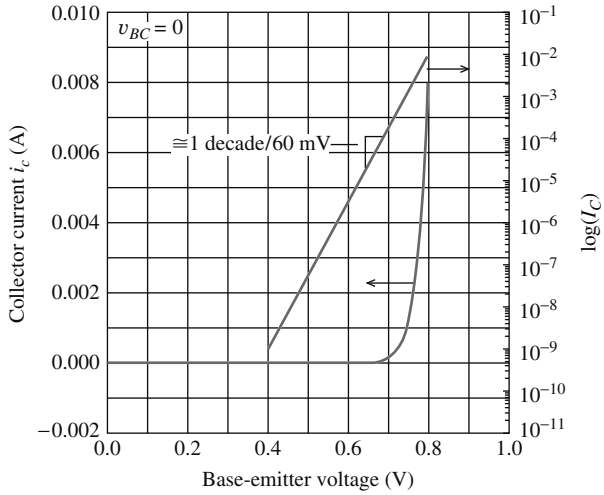


Figure 5.11 BJT transfer characteristic in the forward-active region.

common-emitter current gain, $\beta_R = 5$, to enhance their visibility. As noted earlier, the reverse-current gain β_R is often less than 1.

Using the polarities defined in Fig. 5.9(b) for the *pnp* transistor, the output characteristics will appear exactly the same as in Fig. 5.10, except that the horizontal axis will be the voltage v_{EC} rather than v_{CE}. Remember that $i_B > 0$ and $i_C > 0$ correspond to currents exiting the base and collector terminals of the *pnp* transistor.

5.5.2 TRANSFER CHARACTERISTICS

The **common-emitter transfer characteristic** of the BJT defines the relationship between the collector current and the base-emitter voltage of the transistor. An example of the transfer characteristic for an *npn* transistor is shown in graphical form in Fig. 5.11, with both linear and semilog scales for the particular case of $v_{BC} = 0$. The transfer characteristic is virtually identical to that of a *pn* junction diode. This behavior can also be expressed mathematically by setting $v_{BC} = 0$ in the collector-current expression in Eq. (5.13):

$$i_C = I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \tag{5.20}$$

Because of the exponential relationship in Eq. (5.20), the semilog plot exhibits the same slope as that for a *pn* junction diode. Only a 60-mV change in v_{BE} is required to change the collector current by a factor of 10, and for a fixed collector current, the base-emitter voltage of the silicon BJT will exhibit a -1.8-mV/°C temperature coefficient, just as for the silicon diode (see Sec. 3.5).

EXERCISE: What base-emitter voltage V_{BE} corresponds to $I_C = 100\ \mu$A in an *npn* transistor at room temperature if $I_S = 10^{-16}$ A? For $I_C = 1$ mA?

ANSWERS: 0.691 V; 0.748 V

5.6 THE OPERATING REGIONS OF THE BIPOLAR TRANSISTOR

In the bipolar transistor, each *pn* junction may be independently forward-biased or reverse-biased, so there are four possible regions of operation, as defined in Table 5.2. The operating point establishes the region of operation of the transistor and can be defined by any two of the four terminal voltages

TABLE 5.2
Regions of Operation of the Bipolar Transistor

BASE-EMITTER JUNCTION	BASE-COLLECTOR JUNCTION	
	Reverse Bias	**Forward Bias**
Forward Bias	**Forward-active region** (Normal-active region) (Good amplifier)	**Saturation region*** (Closed switch)
Reverse Bias	**Cutoff region** (Open switch)	**Reverse-active region** (Inverse-active region) (Poor amplifier)

* It is important to note that the saturation region of the bipolar transistor does *not* correspond to the saturation region of the FET. This unfortunate use of terms is historical in nature and something we just have to accept.

or currents. The characteristics of the transistor are quite different for each of the four regions of operation, and in order to simplify our circuit analysis task, we need to be able to make an educated guess as to the region of operation of the BJT.

When both junctions are reverse-biased, the transistor is essentially nonconducting or *cut off* (**cutoff region**) and can be considered an open switch. If both junctions are forward-biased, the transistor is operating in the **saturation region** and appears as a closed switch. Cutoff and saturation are most often used to represent the two states in binary logic circuits implemented with BJTs. For example, switching between these two operating regions occurs in the transistor-transistor logic circuits that we shall study in Chapter 9 on bipolar logic circuits.

In the **forward-active region** (also called the **normal-active region** or **just active region**), in which the base-emitter junction is forward-biased and the base-collector junction is reverse-biased, the BJT can provide high current, voltage, and power gains. The forward-active region is most often used to achieve high-quality amplification. In addition, in the fastest form of bipolar logic, called emitter-coupled logic, the transistors switch between the cutoff and the forward-active regions.

In the **reverse-active region** (or **inverse-active region**), the base-emitter junction is reverse-biased and the base-collector junction is forward-biased. In this region, the transistor exhibits low current gain, and the reverse-active region is not often used. However, we will see an important application of the reverse-active region in transistor-transistor logic circuits in Chapter 9. Reverse operation of the bipolar transistor has also found use in analog-switching applications.

The transport model equations describe the behavior of the bipolar transistor for any combination of terminal voltages and currents. However, the complete sets of equations in (5.13) and (5.17) are quite imposing. In subsequent sections, bias conditions specific to each of the four regions of operation will be used to obtain simplified sets of relationships that are valid for the individual regions. The Q-point for the BJT is (I_C, V_{CE}) for the *npn* transistor and (I_C, V_{EC}) for the *pnp*.

EXERCISE: What is the region of operation of (a) an *npn* transistor with $V_{BE} = 0.75$ V and $V_{BC} = -0.70$ V? (b) A *pnp* transistor with $V_{CB} = 0.70$ V and $V_{EB} = 0.75$ V?

ANSWERS: Forward-active region; saturation region

5.7 TRANSPORT MODEL SIMPLIFICATIONS

The complete sets of transport model equations developed in Secs. 5.2 and 5.3 describe the behavior of the *npn* and *pnp* transistors for any combination of terminal voltages and currents, and these

equations are indeed the basis for the models used in SPICE circuit simulation. However, the full sets of equations are quite imposing. Now we will explore simplifications that can be used to reduce the complexity of the model descriptions for each of the four different regions of operation identified in Table 5.2.

5.7.1 SIMPLIFIED MODEL FOR THE CUTOFF REGION

The easiest region to understand is the cutoff region, in which both junctions are reverse-biased. For an *npn* transistor, the cutoff region requires $v_{BE} \leq 0$ and $v_{BC} \leq 0$. Let us further assume that

$$v_{BE} < -\frac{4kT}{q} \qquad \text{and} \qquad v_{BC} < -4\frac{kT}{q} \qquad \text{where } -4\frac{kT}{q} = -0.1\text{V}$$

These two conditions allow us to neglect the exponential terms in Eq. (5.13), yielding the following simplified equations for the *npn* terminal currents in cutoff:

$$\begin{aligned} i_C &= I_S\left[\cancel{\exp\left(\frac{v_{BE}}{V_T}\right)}^{0} - \cancel{\exp\left(\frac{v_{BC}}{V_T}\right)}^{0}\right] - \frac{I_S}{\beta_R}\left[\cancel{\exp\left(\frac{v_{BC}}{V_T}\right)}^{0} - 1\right] \\ i_E &= I_S\left[\cancel{\exp\left(\frac{v_{BE}}{V_T}\right)}^{0} - \cancel{\exp\left(\frac{v_{BC}}{V_T}\right)}^{0}\right] + \frac{I_S}{\beta_F}\left[\cancel{\exp\left(\frac{v_{BE}}{V_T}\right)}^{0} - 1\right] \\ i_B &= \frac{I_S}{\beta_F}\left[\cancel{\exp\left(\frac{v_{BE}}{V_T}\right)}^{0} - 1\right] + \frac{I_S}{\beta_R}\left[\cancel{\exp\left(\frac{v_{BC}}{V_T}\right)}^{0} - 1\right] \end{aligned} \tag{5.21}$$

or

$$i_C = +\frac{I_S}{\beta_R} \qquad i_E = -\frac{I_S}{\beta_F} \qquad i_B = -\frac{I_S}{\beta_F} - \frac{I_S}{\beta_R}$$

In cutoff, the three terminal currents — i_C, i_E, and i_B — are all constant and smaller than the saturation current I_S of the transistor. The simplified model for this situation is shown in Fig. 5.12(b). In cutoff, only very small leakage currents appear in the three transistor terminals. In most cases, these currents are negligibly small and can be assumed to be zero.

We usually think of the transistor operating in the cutoff region as being "off" with essentially zero terminal currents, as indicated by the three-terminal open-circuit model in Fig. 5.12(c). The cutoff region represents an open switch and is used as one of the two states required for binary logic circuits.

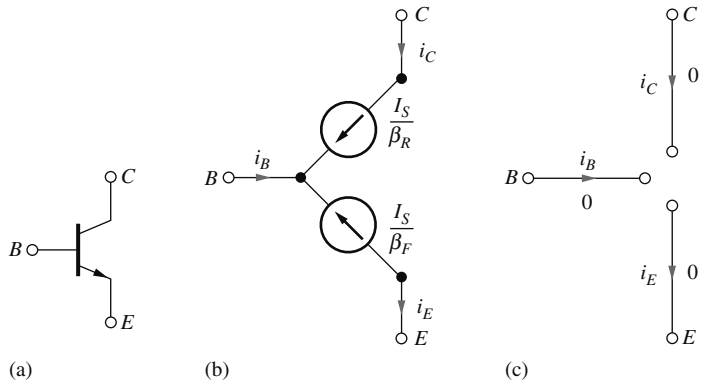


Figure 5.12 Modeling the *npn* transistor in cutoff: (a) *npn* transistor, (b) constant leakage current model, (c) open-circuit model.

EXAMPLE 5.2 A BJT BIASED IN CUTOFF

Cutoff represents the "off state" in switching applications, so an understanding of the magnitudes of the currents involved is important. In this example, we explore how closely the "off state" approaches zero.

PROBLEM Figure 5.13 is an example of a circuit in which the transistor is biased in the cutoff region. Estimate the currents using the simplified model in Fig. 5.12, and compare to calculations using the full transport model.

SOLUTION **Known Information and Given Data:** From the figure, $I_S = 10^{-16}$ A, $\alpha_F = 0.95$, $\alpha_R = 0.25$, $V_{BE} = 0$ V, $V_{BC} = -5$ V

Unknowns: I_C, I_B, I_E

Approach: First analyze the circuit using the simplified model of Fig. 5.12. Then, compare the results to calculations using the voltages to simplify the transport equations.

Assumptions: $V_{BE} = 0$ V, so the "diode" terms containing V_{BE} are equal to 0. $V_{BC} = -5$ V, which is much less than $-4kT/q = -100$ mV, so the transport model equations can be simplified.

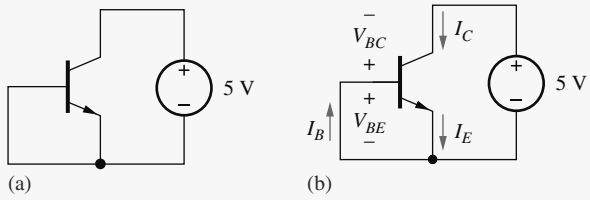


Figure 5.13 (a) *npn* transistor bias in the cutoff region (for calculations, use $I_S = 10^{-16}$ A, $\alpha_F = 0.95$, $\alpha_R = 0.25$); (b) normal current directions.

Analysis: The voltages $V_{BE} = 0$ and $V_{BC} = -5$ V are consistent with the definition of the cutoff region. If we use the open-circuit model in Fig. 5.12(c), the currents I_C, I_E, and I_B are all predicted to be zero.

To obtain a more exact estimate of the currents, we use the transport model equations. For the circuit in Fig. 5.13, the base-emitter voltage is exactly zero, and $V_{BC} \ll 0$. Therefore, Eq. (5.13) reduces to

$$I_C = I_S\left(1 + \frac{1}{\beta_R}\right) = \frac{I_S}{\alpha_R} = \frac{10^{-16}\text{ A}}{0.25} = 4 \times 10^{-16}\text{ A}$$

$$I_E = I_S = 10^{-16}\text{ A} \qquad \text{and} \qquad I_B = -\frac{I_S}{\beta_R} = -\frac{10^{-16}\text{ A}}{\frac{1}{3}} = -3 \times 10^{-16}\text{ A}$$

The calculated currents in the terminals are very small but nonzero. Note, in particular, that the base current is not zero and that small currents exit both the emitter and base terminals of the transistor.

Check of Results: As a check on our results, we see that Kirchhoff's current law is satisfied for the transistor treated as a super node: $i_C + i_B = i_E$.

Discussion: The voltages $V_{BE} = 0$ and $V_{BC} = -5$ V are consistent with the definition of the cutoff region. Thus, we expect the currents to be negligibly small. Here again we see an example of the use of different levels of modeling to achieve different degrees of precision in the answer $[(I_C, I_E, I_B) = (0, 0, 0)$ or $(4 \times 10^{-16}$ A, 10^{-16} A, -3×10^{-16} A)].

EXERCISE: Calculate the values of the currents in the circuit in Fig. 5.13(a).(a) if the value of the voltage source is changed to 10 V and (b) if the base-emitter voltage is set to −3 V using a second voltage source.

ANSWERS: (a) No change; (b) 0.300 fA, 5.26 aA, −0.305 fA

5.7.2 MODEL SIMPLIFICATIONS FOR THE FORWARD-ACTIVE REGION

Arguably the most important region of operation of the BJT is the forward-active region, in which the emitter-base junction is forward-biased and the collector-base junction is reverse-biased. In this region, the transistor can exhibit high voltage and current gains and is useful for analog amplification. From Table 5.2, we see that the forward-active region of an *npn* transistor corresponds to $v_{BE} \geq 0$ and $v_{BC} \leq 0$. In most cases, the forward-active region will have

$$v_{BE} > 4\frac{kT}{q} = 0.1 \text{ V} \qquad \text{and} \qquad v_{BC} < -4\frac{kT}{q} = -0.1 \text{ V}$$

and we can assume that $\exp(-v_{BC}/V_T) \ll 1$ just as we did in simplifying Eq. set (5.21). We can also assume $\exp(v_{BE}/V_T) \gg 1$. These simplifications yield

$$\begin{aligned} i_C &= I_S \exp\left(\frac{v_{BE}}{V_T}\right) + \frac{I_S}{\beta_R} \\ i_E &= \frac{I_S}{\alpha_F} \exp\left(\frac{v_{BE}}{V_T}\right) + \frac{I_S}{\beta_F} \\ i_B &= \frac{I_S}{\beta_F} \exp\left(\frac{v_{BE}}{V_T}\right) - \frac{I_S}{\beta_F} - \frac{I_S}{\beta_R} \end{aligned} \tag{5.22}$$

The exponential term in each of these expressions is usually huge compared to the other terms. By neglecting the small terms, we find the most useful simplifications of the BJT model for the forward-active region:

$$i_C = I_S \exp\left(\frac{v_{BE}}{V_T}\right) \qquad i_E = \frac{I_S}{\alpha_F} \exp\left(\frac{v_{BE}}{V_T}\right) \qquad i_B = \frac{I_S}{\beta_F} \exp\left(\frac{v_{BE}}{V_T}\right) \tag{5.23}$$

In these equations, the fundamental, exponential relationship between all the terminal currents and the base-emitter voltage v_{BE} is once again clear. In the forward-active region, the terminal currents all have the form of diode currents in which the controlling voltage is the base-emitter junction potential. It is also important to note that the currents are all independent of the base-collector voltage v_{BC}. The collector current i_C can be modeled as a voltage-controlled current source that is controlled by the base-emitter voltage and independent of the collector voltage.

By taking ratios of the terminal currents in Eq. (5.23), two important auxiliary relationships for the forward-active region are found, and observing that $i_E = i_C + i_B$ yields a third important result:

$$i_C = \alpha_F i_E \qquad \text{and} \qquad i_C = \beta_F i_B \qquad i_E = (\beta_F + 1) i_B \tag{5.24}$$

The results from Eq. (5.24) are placed in a circuit context in the next two examples from Fig. 5.14.

DESIGN NOTE **FORWARD-ACTIVE REGION**

Operating points in the forward-active region are normally used for linear amplifiers. Our dc model for the forward-active region is quite simple:

$$I_C = \beta_F I_B \qquad \text{and} \qquad I_E = (\beta_F + 1) I_B \quad \text{with} \quad V_{BE} \cong 0.7 \text{ V}.$$

Forward-active operation requires $V_{BE} > 0$ and $V_{CE} \geq V_{BE}$.

EXAMPLE 5.3 FORWARD-ACTIVE REGION OPERATION WITH EMITTER CURRENT BIAS

Current sources are widely utilized for biasing in circuit design, and such a source is used to set the Q-point current in the transistor in Fig. 5.14(a).

PROBLEM Find the emitter, base and collector currents, and base-emitter voltage for the transistor biased by a current source in Fig. 5.14(a).

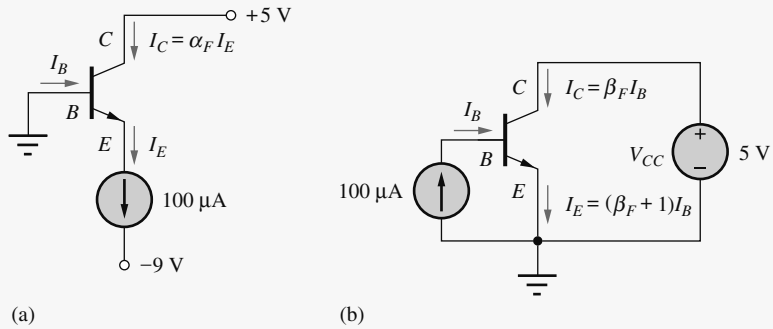


Figure 5.14 Two *npn* transistors operating in the forward-active region ($I_S = 10^{-16}$ A and $\alpha_F = 0.95$ are assumed for the example calculations).

SOLUTION **Known Information and Given Data:** An *npn* transistor biased by the circuit in Fig. 5.14(a) with $I_S = 10^{-16}$ A and $\alpha_F = 0.95$. From the circuit, $V_{BC} = V_B - V_C = -5$ V and $I_E = +100$ μA.

Unknowns: I_C, I_B, V_{BE}

Approach: Show that the transistor is in the forward-active region of operation and use Eqs. (5.23) and (5.24) to find the unknown currents and voltage.

Assumptions: Room temperature operation with $V_T = 25.0$ mV

Analysis: From the circuit, we observe that the emitter current is forced by the current source to be $I_E = +100$ μA, and the current source will forward-bias the base-emitter diode. Study of the mathematical model in Eq. (5.13) also confirms that the base-emitter voltage must be positive (forward bias) in order for the emitter current to be positive. Thus, we have $V_{BE} > 0$ and $V_{BC} < 0$, which correspond to the forward-active region of operation for the *npn* transistor.

The base and collector currents can be found using Eq. (5.24) with $I_E = 100$ μA:

$$I_C = \alpha_F I_E = 0.95 \cdot 100 \,\mu\text{A} = 95 \,\mu\text{A}$$

Solving for β_F gives $\beta_F = \dfrac{\alpha_F}{1-\alpha_F} = \dfrac{0.95}{1-0.95} = 19 \qquad \beta_F + 1 = 20$

and $I_B = \dfrac{I_E}{\beta_F + 1} = \dfrac{100\ \mu\text{A}}{20} = 5\ \mu\text{A}$

The base-emitter voltage is found from the emitter current expression in Eq. (5.23):

$$V_{BE} = V_T \ln \frac{\alpha_F I_E}{I_S} = (0.025\ \text{V}) \ln \frac{0.95(10^{-4}\text{A})}{10^{-16}\text{A}} = 0.690\ \text{V}$$

Check of Results: As a check on our results, we see that Kirchhoff's current law is satisfied for the transistor treated as a super node: $i_C + i_B = i_E$. Also we can check V_{BE} using both the collector and base current expressions in Eq. (5.23).

Discussion: We see that most of the current being forced or "pulled" out of the emitter by the current source comes directly through the transistor from the collector. This is the common-base mode in which $i_C = \alpha_F i_E$ with $\alpha_F \cong 1$.

EXERCISE: Calculate the values of the currents and base-emitter voltage in the circuit in Fig. 5.14(a) if (a) the value of the voltage source is changed to 10 V and (b) the transistor's common-emitter current gain is increased to 50.

ANSWERS: (a) No change; (b) 100 μA, 1.96 μA, 98.0 μA, 0.690 V

EXAMPLE 5.4 FORWARD-ACTIVE REGION OPERATION WITH BASE CURRENT BIAS

A current source is used to bias the transistor into the forward-active region in Fig. 5.14(b).

PROBLEM Find the emitter, base and collector currents, and base-emitter and base-collector voltages for the transistor biased by the base current source in Fig. 5.14(b).

SOLUTION **Known Information and Given Data:** An *npn* transistor biased by the circuit in Fig. 5.14(b) with $I_S = 10^{-16}$ A and $\alpha_F = 0.95$. From the circuit, $V_C = +5$ V and $I_B = +100\ \mu$A.

Unknowns: I_C, I_B, V_{BE}, V_{BC}

Approach: Show that the transistor is in the forward-active region of operation and use Eqs. (5.23) and (5.24) to find the unknown currents and voltage.

Assumptions: Room temperature operation with $V_T = 25.0$ mV

Analysis: In the circuit in Fig. 5.14(b), base current I_B is now forced to equal 100 μA by the ideal current source. This current enters the base and will exit the emitter, forward-biasing the base-emitter junction. From the mathematical model in Eq. (5.13), we see that positive base current can occur for positive V_{BE} and positive V_{BC}. However, we have $V_{BC} = V_B - V_C = V_{BE} - V_C$. Since the base-emitter diode voltage will be approximately 0.7 V, and $V_C = 5$ V, V_{BC} will be negative (e.g., $V_{BC} \cong 0.7 - 5.0 = -4.3$ V). Thus we have $V_{BE} > 0$ and $V_{BC} < 0$, which corresponds to

the forward-active region of operation for the *npn* transistor, and the collector and emitter currents can be found using Eq. (5.24) with $I_B = 100\ \mu\text{A}$:

$$I_C = \beta_F I_B = 19 \cdot 100\ \mu\text{A} = 1.90\ \text{mA}$$

$$I_E = (\beta_F + 1) I_B = 20 \cdot 100\ \mu\text{A} = 2.00\ \text{mA}$$

The base-emitter voltage can be found from the collector current expression in Eq. (5.23):

$$V_{BE} = V_T \ln \frac{I_C}{I_S} = (0.025\ \text{V}) \ln \frac{1.9 \times 10^{-3}\ \text{A}}{10^{-16}\ \text{A}} = 0.764\ \text{V}$$

$$V_{BC} = V_B - V_C = V_{BE} - V_C = 0.764 - 5 = -4.236\ \text{V}$$

Check of Results: As a check on our results, we see that Kirchhoff's current law is satisfied for the transistor treated as a super node: $i_C + i_B = i_E$. Also we can check the value of V_{BE} using either the emitter or base current expressions in Eq. (5.23). The calculated values of V_{BE} and V_{BC} correspond to forward-active region operation.

Discussion: A large amplification of the current takes place when the current source is injected into the base terminal in Fig. 5.14(b) in contrast to the situation when the source is connected to the emitter terminal in Fig. 5.14(a).

EXERCISE: Calculate the values of the currents and base-emitter voltage in the circuit in Fig. 5.14(b) if (a) the value of the voltage source is changed to 10 V and (b) the transistor's common-emitter current gain is increased to 50.

ANSWERS: (a) No change; (b) 5.00 mA, 100 μA, 5.10 mA, 0.789 V, −4.21 V

EXERCISE: What is the minimum value of V_{CC} that corresponds to forward-active region bias in Fig. 5.14(b)?

ANSWER: $V_{BE} = 0.764$ V

As illustrated in Examples 5.3 and 5.4, Eq. (5.24) can often be used to greatly simplify the analysis of circuits operating in the forward-active region. However, remember this caveat well: **The results in Eq. (5.24) are valid *only* for the forward-active region of operation!**

The BJT is often considered a current-controlled device. However, from Eq. (5.23), we see that the fundamental physics-based behavior of the BJT in the forward-active region is that of a (nonlinear) voltage-controlled current source. The base current should be considered as an unwanted defect current that must be supplied to the base in order for the transistor to operate. In an ideal BJT, β_F would be infinite, the base current would be zero, and the collector and emitter currents would be identical, just as for the FET. (Unfortunately, it is impossible to fabricate such a BJT.)

Equation (5.23) leads to the simplified circuit model for the forward-active region shown in Fig. 5.15. The current in the base-emitter diode is amplified by the common-emitter current gain β_F and appears in the collector terminal. However, remember that the base and collector currents are exponentially related to the base-emitter voltage. Because the base-emitter diode is forward-biased in the forward-active region, the transistor model of Fig. 5.15(b) can be further simplified to that of Fig. 5.15(c), in which the diode is replaced by its constant voltage drop (CVD) model, in this

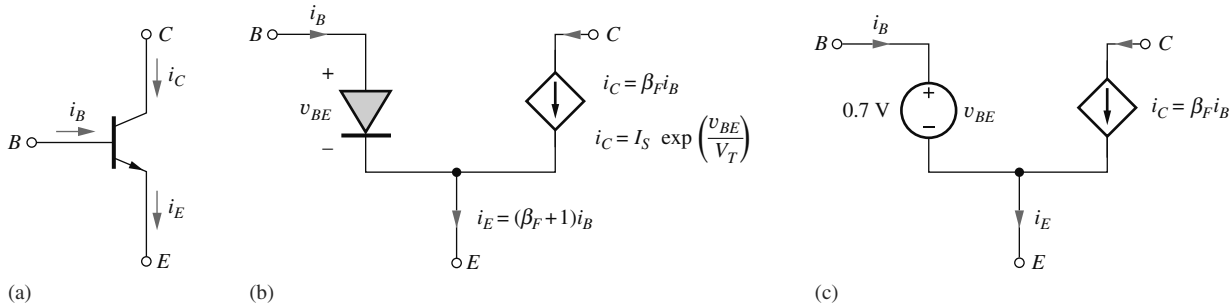


Figure 5.15 (a) *npn* transistor; (b) simplified model for the forward-active region; (c) further simplification for the forward-active region using the CVD model for the diode.

case $V_{BE} = 0.7$ V. The dc base and emitter voltages differ by the 0.7-V diode voltage drop in the forward-active region.

EXAMPLE 5.5 FORWARD-ACTIVE REGION BIAS USING TWO POWER SUPPLIES

Analog circuits frequently operate from a pair of positive and negative power supplies so that bipolar input and output signals can easily be accommodated. The circuit in Fig. 5.16 provides one possible circuit configuration in which resistor R and –9-V source replace the current source utilized in Fig. 5.14(a). Collector resistor R_C has been added to reduce the collector-emitter voltage.

PROBLEM Find the Q-point for the transistor in the circuit in Fig. 5.16.

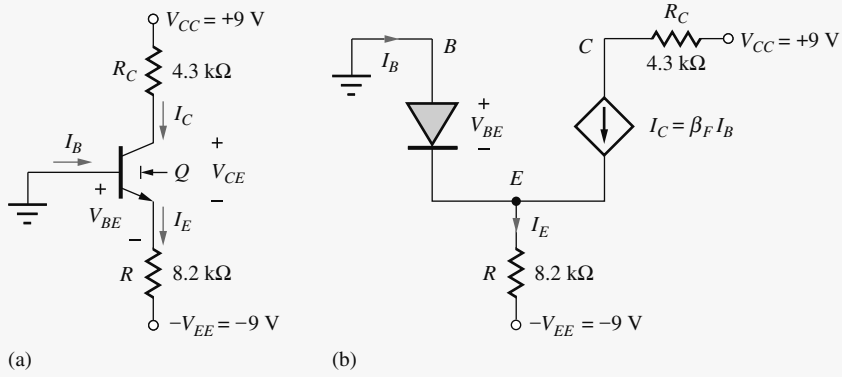


Figure 5.16 (a) *npn* Transistor circuit (assume $\beta_F = 50$ and $\beta_R = 1$); (b) simplified model for the forward-active region.

SOLUTION **Known Information and Given Data:** *npn* transistor in the circuit in Fig. 5.16(a) with $\beta_F = 50$ and $\beta_R = 1$

Unknowns: Q-point (I_C, V_{CE})

Approach: In this circuit, the base-collector junction will tend to be reverse-biased by the 9-V source. The combination of the resistor and the –9-V source will force a current out of the emitter and forward-bias the base-emitter junction. Thus, the transistor appears to be biased in the forward-active region of operation.

Assumptions: Assume forward-active region operation; since we do not know the saturation current, assume $V_{BE} = 0.7$ V; use the simplified model for the forward-active region to analyze the circuit as in Fig. 5.16(b).

Analysis: The currents can now be found by using KVL around the base-emitter loop:

$$V_{BE} + 8200I_E - V_{EE} = 0$$

For $V_{BE} = 0.7$ V, $0.7 + 8200I_E - 9 = 0$ or $I_E = \dfrac{8.3 \text{ V}}{8200\ \Omega} = 1.01$ mA

At the emitter node, $I_E = (\beta_F + 1)I_B$, so

$$I_B = \frac{1.01 \text{ mA}}{50 + 1} = 19.8\ \mu\text{A} \qquad \text{and} \qquad I_C = \beta_F I_B = 0.990 \text{ mA}$$

The collector-emitter voltage is equal to

$$V_{CE} = V_{CC} - I_C R_C - (-V_{BE}) = 9 - .990 \text{ mA}(4.3 \text{ k}\Omega) + 0.7 = 5.44 \text{ V}$$

The Q-point is (0.990 mA, 5.44 V).

Check of Results: We see that KVL is satisfied around the output loop containing the collector-emitter voltage: $+9 - V_{RC} - V_{CE} - V_R - (-9) = 9 - 4.3 - 5.4 - 8.3 + 9 = 0$. We must check the forward-active region assumption $V_{CE} = 5.4$ V which is greater than $V_{BE} = 0.7$ V. Also, the currents are all positive and $I_C + I_B = I_E$.

Discussion: In this circuit, the combination of the resistor and the −9-V source replace the current source that was used to bias the transistor in Fig. 5.14(a).

Computer-Aided Analysis: SPICE contains a built-in model for the bipolar transistor that will be discussed in detail in Sec. 5.10. SPICE simulation with the default *npn* transistor model yields a Q-point that agrees well with our hand analysis: (0.993 mA, 5.50 V).

EXERCISE: **(a) Find the Q-point in Ex. 5.5 if resistor *R* is changed to 5.6 kΩ. (b) What value of *R* is required to set the current to approximately 100 μA in the original circuit?**

ANSWERS: **(a) (1.45 mA, 3.5 V); (b) 82 kΩ.**

Figure 5.17 displays the results of simulation of the collector current of the transistor in Fig. 5.16 versus the supply voltage V_{CC}. For $V_{CC} > 0$, the collector-base junction will be reverse-biased, and the transistor will be in the forward-active region. In this region, the circuit behaves essentially as a 1-mA ideal current source in which the output current is independent of V_{CC}. Note that the circuit actually behaves as a current source for V_{CC} down to approximately −0.5 V. By the definitions in Table 5.2, the transistor enters saturation for $V_{CC} < 0$, but the transistor does not actually enter heavy saturation until the base-collector junction begins to conduct for $V_{BC} \geq +0.5$ V.

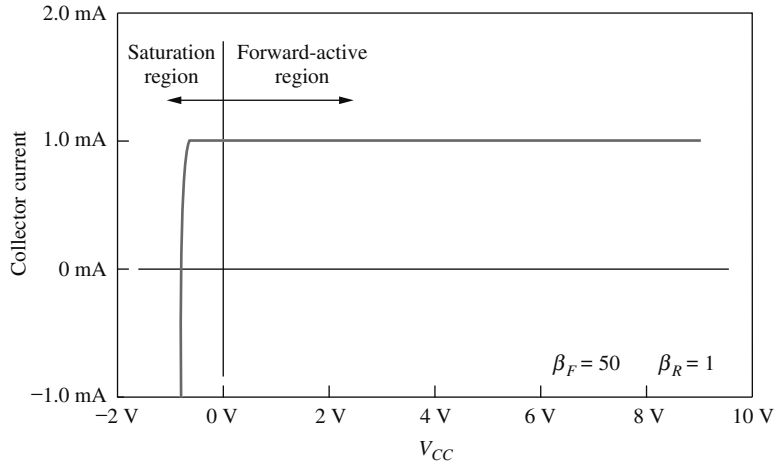


Figure 5.17 Simulation of output characteristics of circuit of Fig. 5.16(a).

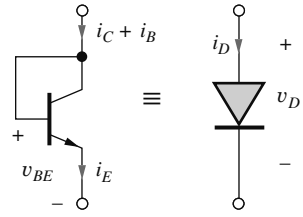


Figure 5.18 Diode-connected transistor.

EXERCISE: Find the three terminal currents in the transistor in Fig. 5.16 if the 8.2 kΩ resistor value is changed to 5.6 kΩ.

ANSWERS: 1.48 mA, 29.1 μA, 1.45 mA

EXERCISE: What are the actual values of V_{BE} and V_{CE} for the transistor in Fig. 5.16(a) if $I_S = 5 \times 10^{-16}$ A? (Note that an iterative solution is necessary.)

ANSWERS: 0.708 V, 5.44 V

5.7.3 DIODES IN BIPOLAR INTEGRATED CIRCUITS

In integrated circuits, we often want the characteristics of a diode to match those of the BJT as closely as possible. In addition, it takes about the same amount of area to fabricate a diode as a full bipolar transistor. For these reasons, a diode is usually formed by connecting the base and collector terminals of a bipolar transistor, as shown in Fig. 5.18. This connection forces $v_{BC} = 0$.

Using the transport model equations for BJT with this boundary condition yields an expression for the terminal current of the "diode":

$$i_D = (i_C + i_B) = \left(I_S + \frac{I_S}{\beta_F}\right)\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] = \frac{I_S}{\alpha_F}\left[\exp\left(\frac{v_D}{V_T}\right) - 1\right] \qquad (5.25)$$

The terminal current has an i-v characteristic corresponding to that of a diode with a reverse saturation current that is determined by the BJT parameters. This technique is often used in both analog and digital circuit design; we will see many examples of its use in the analog designs in Part III.

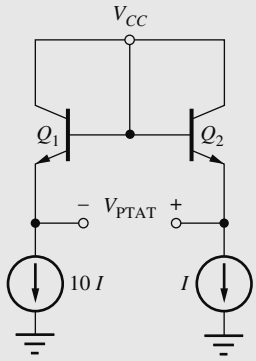
EXERCISE: What is the equivalent saturation current of the diode in Fig 5.18 if the transistor is described by $I_S = 2 \times 10^{-14}$ A and $\alpha_F = 0.95$?

ANSWER: 21 fA

ELECTRONICS IN ACTION

The Bipolar Transistor PTAT Cell

The diode version of the PTAT cell that generates an output voltage **p**roportional **t**o **a**bsolute **t**emperature was introduced back in Chapter 3. We can also easily implement the PTAT cell using two bipolar transistors as shown in the figure here in which two identical bipolar transistors are biased in the forward-active region by current sources with a 10:1 current ratio.



Logo © *Auburn University*

The PTAT voltage is given by

$$V_{\text{PTAT}} = V_{E2} - V_{E1} = (V_{CC} - V_{BE2}) - (V_{CC} - V_{BE1}) = V_{BE1} - V_{BE2}$$

$$V_{\text{PTAT}} = V_T \ln\left(\frac{10I}{I_S}\right) - V_T \ln\left(\frac{I}{I_S}\right) = \frac{kT}{q}\ln(10) \quad \text{and} \quad \frac{\mathrm{d}V_{\text{PTAT}}}{\mathrm{d}T} = \frac{198\ \mu V}{^\circ K}$$

The bipolar PTAT cell is the circuit most commonly used in electronic thermometry.

5.7.4 SIMPLIFIED MODEL FOR THE REVERSE-ACTIVE REGION

In the reverse-active region, also called the inverse-active region, the roles of the emitter and collector terminals are reversed. The base-collector diode is forward-biased and the base-emitter junction is reverse-biased, and we can assume that $\exp(v_{BE}/V_T) \ll 1$ for $v_{BE} < -0.1$ V just as we did in simplifying Eq. set (5.21). Applying this approximation to Eq. (5.13) and neglecting the -1 terms relative to the exponential terms yields the simplified equations for the reverse-active region:

$$i_C = -\frac{I_S}{\alpha_R}\exp\left(\frac{v_{BC}}{V_T}\right) \qquad i_E = -I_S \exp\left(\frac{v_{BC}}{V_T}\right) \qquad i_B = \frac{I_S}{\beta_R}\exp\left(\frac{v_{BC}}{V_T}\right) \tag{5.26}$$

Ratios of these equations yield $i_E = -\beta_R i_B$ and $i_E = \alpha_R i_C$.

Equation (5.26) leads to the simplified circuit model for the reverse-active region shown in Fig. 5.19. The base current in the base-collector diode is amplified by the reverse common-emitter current gain β_R and enters the emitter terminal.

In the reverse-active region, the base-collector diode is now forward-biased, and the transistor model of Fig. 5.19(b) can be further simplified to that of Fig. 5.19(c), in which the diode is replaced by its CVD model with a voltage of 0.7 V. The base and collector voltages differ only by one 0.7-V diode drop in the reverse-active region.

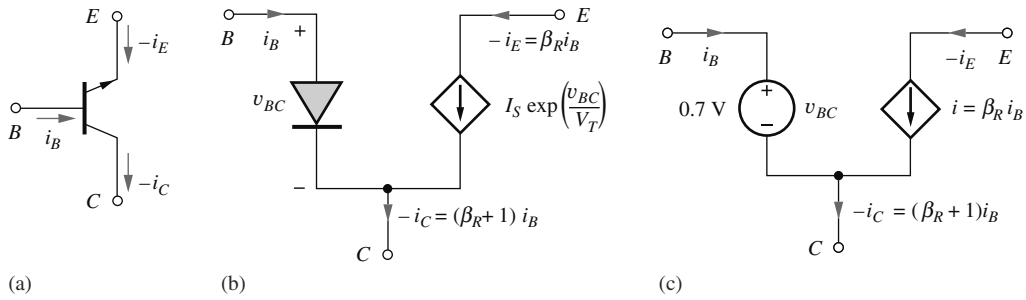


Figure 5.19 (a) *npn* transistor in the reverse-active region; (b) simplified circuit model for the reverse-active region; (c) further simplification in the reverse-active region using the CVD model for the diode.

EXAMPLE 5.6 REVERSE-ACTIVE REGION ANALYSIS

Although the reverse-active region is not often used, one does encounter it fairly frequently in the laboratory. If the transistor is inadvertently plugged in upside down, for example, the transistor will be operating in the reverse-active region. On the surface, the circuit will seem to be working but not very well. It is useful to be able to recognize when this error has occurred.

PROBLEM The collector and emitter terminals of the *npn* transistor in Fig. 5.16 have been interchanged in the circuit in Fig. 5.20 (perhaps the transistor was plugged into the circuit backwards by accident). Find the new Q-point for the transistor in the circuit in Fig. 5.20.

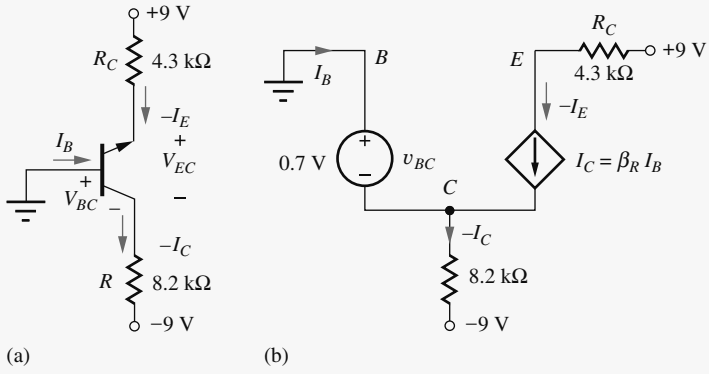


Figure 5.20 (a) Circuit of Fig. 5.16 with *npn* transistor orientation reversed; (b) circuit simplification using the model for the reverse-active region (analysis of the circuit uses $\beta_F = 50$ and $\beta_R = 1$).

SOLUTION **Known Information and Given Data:** *npn* transistor in the circuit in Fig. 5.20 with $\beta_F = 50$ and $\beta_R = 1$

Unknowns: Q-point (I_C, V_{CE})

Approach: In this circuit, the base-emitter junction is reverse-biased by the 9-V source ($V_{BE} = V_B - V_E = -9$ V). The combination of the 8.2-kΩ resistor and the −9-V source will pull a current *out of* the collector and forward-bias the base-collector junction. Thus, the transistor appears to be biased in the reverse-active region of operation.

Assumptions: Assume reverse-active region operation; since we do not know the saturation current, assume $V_{BC} = 0.7$ V; use the simplified model for the reverse-active region to analyze the circuit as in Fig. 5.20(b).

Analysis: The current exiting from the collector $(-I_C)$ is now equal to

$$(-I_C) = \frac{-0.7\text{ V} - (-9\text{ V})}{8200\ \Omega} = 1.01\text{ mA}$$

The current through the 8.2-kΩ resistor is unchanged compared to that in Fig. 5.16. However, significant differences exist in the currents in the base terminal and the +9-V source. At the collector node, $(-I_C) = (\beta_R + 1)I_B$, and at the emitter, $(-I_E) = \beta_R I_B$:

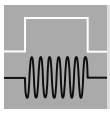
$$I_B = \frac{1.01\text{ mA}}{2} = 0.505\text{ mA} \qquad \text{and} \qquad -I_E = (1)I_B = 0.505\text{ mA}$$

$$V_{EC} = 9 - 4300(0.505\text{ mA}) - (-0.7\text{ V}) = 7.5\text{ V}$$

Check of Results: We see that KVL is satisfied around the output loop containing the collector-emitter voltage: $+9 - V_{CE} - V_R - (-9) = 9 - 9.7 - 8.3 + 9 = 0$. Also, $I_C + I_B = I_E$, and the calculated current directions are all consistent with the assumption of reverse-active region operation. Finally $V_{EB} = 9 - 43\text{ k}\Omega\ (0.505\text{ mA}) = 6.8\text{ V}$. $V_{EB} > 0\text{ V}$, and the reverse active assumption is correct.

Discussion: Note that the base current is much larger than expected, whereas the current entering the upper terminal of the device is much smaller than would be expected if the transistor were in the circuit as originally drawn in Fig. 5.16. These significant differences in current often lead to unexpected shifts in voltage levels at the base and collector terminals of the transistor in more complicated circuits.

Computer-Aided Design: The built-in SPICE model is valid for any operating region, and simulation with the default model gives results very similar to hand calculations.



DESIGN NOTE **REVERSE-ACTIVE REGION CHARACTERISTICS**

Note that the currents for reverse-active region operation are usually very different from those found for forward-active region operation in Fig. 5.16. These drastic differences are often useful in debugging circuits that we have built in the lab and can be used to discover transistors that have been improperly inserted into a circuit breadboard.

EXERCISE: Find the three terminal currents in the transistor in Fig. 5.20 if resistor *R* is changed to 5.6 kΩ.

ANSWERS: 1.48 mA, 0.741 mA, 0.741 mA

5.7.5 MODELING OPERATION IN THE SATURATION REGION

The fourth and final region of operation is called the saturation region. In this region, both junctions are forward-biased, and the transistor typically operates with a small voltage between collector and emitter terminals. In the saturation region, the dc value of v_{CE} is called the **saturation voltage** of the transistor: v_{CESAT} for the *npn* transistor or v_{ECSAT} for the *pnp* transistor.

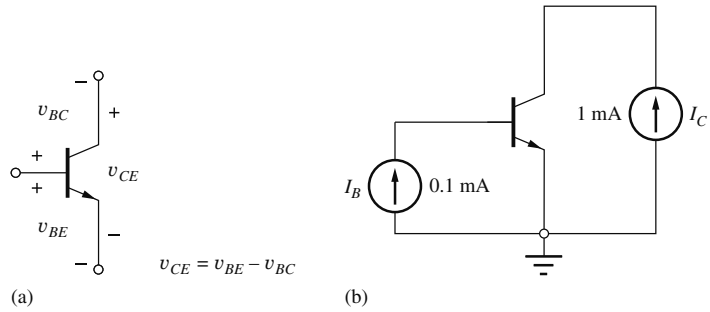


Figure 5.21 (a) Relationship between the terminal voltages of the transistor; (b) circuit for Ex. 5.8.

In order to determine v_{CESAT}, we assume that both junctions are forward-biased so that i_C and i_B from Eq. (5.13) can be approximated as

$$\begin{aligned} i_C &= I_S \exp\left(\frac{v_{BE}}{V_T}\right) - \frac{I_S}{\alpha_R}\exp\left(\frac{v_{BC}}{V_T}\right) \\ i_B &= \frac{I_S}{\beta_F}\exp\left(\frac{v_{BE}}{V_T}\right) + \frac{I_S}{\beta_R}\exp\left(\frac{v_{BC}}{V_T}\right) \end{aligned} \tag{5.27}$$

Simultaneous solution of these equations using $\beta_R = \alpha_R/(1-\alpha_R)$ yields expressions for the base-emitter and base-collector voltages:

$$v_{BE} = V_T \ln \frac{i_B + (1-\alpha_R)i_C}{I_S\left[\frac{1}{\beta_F} + (1-\alpha_R)\right]} \quad \text{and} \quad v_{BC} = V_T \ln \frac{i_B - \frac{i_C}{\beta_F}}{I_S\left[\frac{1}{\alpha_R}\right]\left[\frac{1}{\beta_F} + (1-\alpha_R)\right]} \tag{5.28}$$

By applying KVL to the transistor in Fig. 5.21, we find that the collector-emitter voltage of the transistor is $v_{CE} = v_{BE} - v_{BC}$, and substituting the results from Eq. (5.28) into this equation yields an expression for the saturation voltage of the *npn* transistor:

$$v_{\text{CESAT}} = V_T \ln\left[\left(\frac{1}{\alpha_R}\right)\frac{1 + \frac{i_C}{(\beta_R+1)i_B}}{1 - \frac{i_C}{\beta_F i_B}}\right] \qquad \text{for } i_B > \frac{i_C}{\beta_F} \tag{5.29}$$

This equation is important and highly useful in the design of saturated digital switching circuits. For a given value of collector current, Eq. (5.29) can be used to determine the base current required to achieve a desired value of v_{CESAT}.

Note that Eq. (5.29) is valid only for $i_B > i_C/\beta_F$. This is an auxiliary condition that can be used to define saturation region operation. The ratio i_C/β_F represents the base current needed to maintain transistor operation in the forward-active region. If the base current exceeds the value needed for forward-active region operation, the transistor will enter saturation. The actual value of i_C/i_B is often called the **forced beta $\boldsymbol{\beta_{\text{FOR}}}$** of the transistor, where $\beta_{\text{FOR}} \le \beta_F$.

EXAMPLE 5.7 SATURATION VOLTAGE CALCULATION

The BJT saturation voltage is important in many switching applications including logic circuits and power supplies. Here we find an example of the value of the saturation voltage for a forced beta of 10.

PROBLEM Calculate the saturation voltage for an *npn* transistor with $I_C = 1$ mA, $I_B = 0.1$ mA, $\beta_F = 50$, and $\beta_R = 1$.

SOLUTION **Known Information and Given Data:** An *npn* transistor is operating with $I_C = 1$ mA, $I_B = 0.1$ mA, $\beta_F = 50$, and $\beta_R = 1$

Unknowns: Collector-emitter voltage of the transistor

Approach: Because $I_C/I_B = 10 < \beta_F$, the transistor will indeed be saturated. Therefore we can use Eq. (5.29) to find the saturation voltage.

Assumptions: Room temperature operation with $V_T = 0.025$ V

Analysis: Using $\alpha_R = \beta_R/(\beta_R + 1) = 0.5$ and $I_C/I_B = 10$ yields

$$v_{\text{CESAT}} = (0.025\text{ V}) \ln \left[\left(\frac{1}{0.5} \right) \frac{1 + \dfrac{1\text{ mA}}{2(0.1\text{ mA})}}{1 - \dfrac{1\text{ mA}}{50(0.1\text{ mA})}} \right] = 0.068\text{ V}$$

Check of Results: A small, nearly zero, value of saturation voltage is expected; thus the calculated value appears reasonable.

Discussion: We see that the value of V_{CE} in this example is indeed quite small. However, it is nonzero even for $i_C = 0$ [see Prob. 5.56]! It is impossible to force the forward voltages across both *pn* junctions to be exactly equal, which is a consequence of the asymmetric values of the forward and reverse current gains. The existence of this small voltage "offset" is an important difference between the BJT and the MOSFET. In the case triode region operation of the MOSFET, the voltage between drain and source becomes zero when the drain current is zero.

Computer-Aided Analysis: We can simulate the situation in this example by driving the base of the BJT with one current source and the collector with a second. (This is one of the few circuit situations in which we can force a current into the collector using a current source.) SPICE yields $V_{\text{CESAT}} = 0.070$ V. The default temperature in SPICE is 27°C, and the slight difference in V_T accounts for the difference between SPICE result and our hand calculations.

EXERCISE: What is the saturation voltage in Ex. 5.7 if the base current is reduced to 40 μA?

ANSWER: 99.7 mV

EXERCISE: Use Eq. (5.28) to find V_{BESAT} and V_{BCSAT} for the transistor in Ex. 5.7 if $I_S = 10^{-15}$ A.

ANSWERS: 0.694 V, 0.627 V

Figure 5.22 shows the simplified model for the transistor in saturation in which the two diodes are assumed to be forward-biased and replaced by their respective on-voltages. The forward voltages

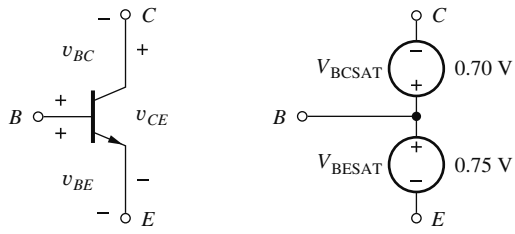
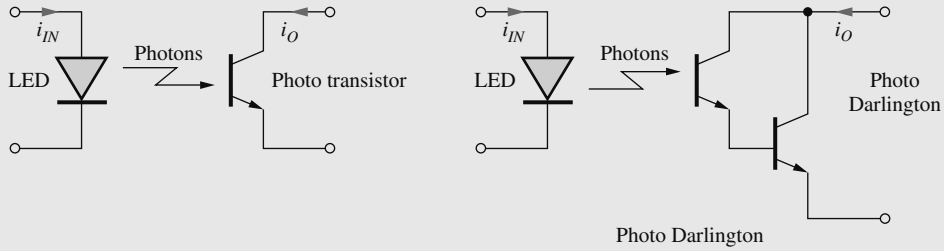


Figure 5.22 Simplified model for the *npn* transistor in saturation.

ELECTRONICS IN ACTION

Optical Isolators

The optical isolator drawn schematically here represents a highly useful circuit that behaves much like a single transistor, but provides a very high breakdown voltage and low capacitance between its input and output terminals. Input current i_{IN} drives a light emitting diode (LED) whose output illuminates the base region of an *npn* transistor. Energy lost by the photons creates hole–electron pairs in the base of the *npn*. The holes represent base current that is then amplified by the current gain β_F of the transistor, whereas the electrons simply become part of the collector current.



The output characteristics of the optical isolator are very similar to those of a BJT operating in the active region in Fig. 5.10. However, the conversion of photons to hole–electron pairs is not very efficient in silicon, and the current transfer ratio, $\beta_F = i_O/i_{IN}$, of the optical isolator is often only around unity. The "Darlington connection" of two transistors (see Sec. 15.2.3), is often used to improve the overall current gain of the isolator. In this case, the output current is increased by the current gain of the second transistor.

The dc isolation provided by such devices can exceed a thousand volts and is limited primarily by the spacing of the pins and the characteristics of the circuit board that the isolator is mounted upon. ac isolation is limited to the low picofarad range by stray capacitance between the input and outputs pins.

of both diodes are normally higher in saturation than in the forward-active region, as indicated in the figure by $V_{\text{BESAT}} = 0.75$ V and $V_{\text{BCSAT}} = 0.7$ V. In this case, V_{CESAT} is 50 mV. In saturation, the terminal currents are determined by the external circuit elements; no simplifying relationships exist between i_C, i_B, and i_E other than $i_C + i_B = i_E$.

5.8 NONIDEAL BEHAVIOR OF THE BIPOLAR TRANSISTOR

As with all devices, the BJT characteristics deviate from our ideal mathematical models in a number of ways. The emitter-base and collector-base diodes that form the bioplar transistor have finite reverse breakdown voltages (see Sec. 3.6.2) that we must carefully consider when choosing a transistor or the power supplies for our circuits. There are also capacitances associated with each of the diodes, and these capacitances place limitations on the high frequency response of the transistor. In addition, we know that holes and electrons in semiconductor materials have finite velocities. Thus, it takes time for the carriers to move from the emitter to the collector, and this time delay places an additional limit on the upper frequency of operation of the bipolar transistor. Finally, the output characteristics of the BJT exhibit a dependence on collector-emitter voltage similar to the channel-length modulation effect that occurs in the MOS transistor (Sec. 4.2.7). This section considers each of these limitations in more detail.

5.8.1 JUNCTION BREAKDOWN VOLTAGES

The bipolar transistor is formed from two back-to-back diodes, each of which has a Zener breakdown voltage associated with it. If the reverse voltage across either *pn* junction is too large, the corresponding diode will break down. In the transistor structure in Fig. 5.1, the emitter region is the most heavily doped region and the collector is the most lightly doped region. These doping differences lead to a relatively low breakdown voltage for the base-emitter diode, typically in the range of 3 to 10 V. On the other hand, the collector-base diode can be designed to break down at much larger voltages. Transistors can be fabricated with collector-base breakdown voltages as high as several hundred volts.[8]

Transistors must be selected with breakdown voltages commensurate with the reverse voltages that will be encountered in the circuit. In the forward-active region, for example, the collector-base junction is operated under reverse bias and must not break down. In the cutoff region, both junctions are reverse-biased, and the relatively low breakdown voltage of the emitter-base junction must not be exceeded.

5.8.2 MINORITY-CARRIER TRANSPORT IN THE BASE REGION

Current in the BJT is predominantly determined by the transport of *minority carriers* across the base region. In the *npn* transistor in Fig. 5.23, transport current i_T results from the diffusion of minority carriers — electrons in the *npn* transistor or holes in the *pnp* — across the base. Base current i_B is composed of hole injection back into the emitter and collector, as well as a small additional current I_{REC} needed to replenish holes lost to recombination with electrons in the base. These three components of base current are shown in Fig. 5.23(a).

An expression for the transport current i_T can be developed using our knowledge of carrier diffusion and the values of base-emitter and base-collector voltages. It can be shown from device physics (beyond the scope of this text) that the voltages applied to the base-emitter and base-collector junctions define the minority-carrier concentrations at the two ends of the base region through these relationships:

$$n(0) = n_{bo} \exp\left(\frac{v_{BE}}{V_T}\right) \qquad \text{and} \qquad n(W_B) = n_{bo} \exp\left(\frac{v_{BC}}{V_T}\right) \tag{5.30}$$

in which $\boldsymbol{n_{bo}}$ is the **equilibrium electron density** in the *p*-type base region.

The two junction voltages establish a minority-carrier concentration gradient across the base region, as illustrated in Fig. 5.23(b). For a narrow base, the minority-carrier density decreases linearly

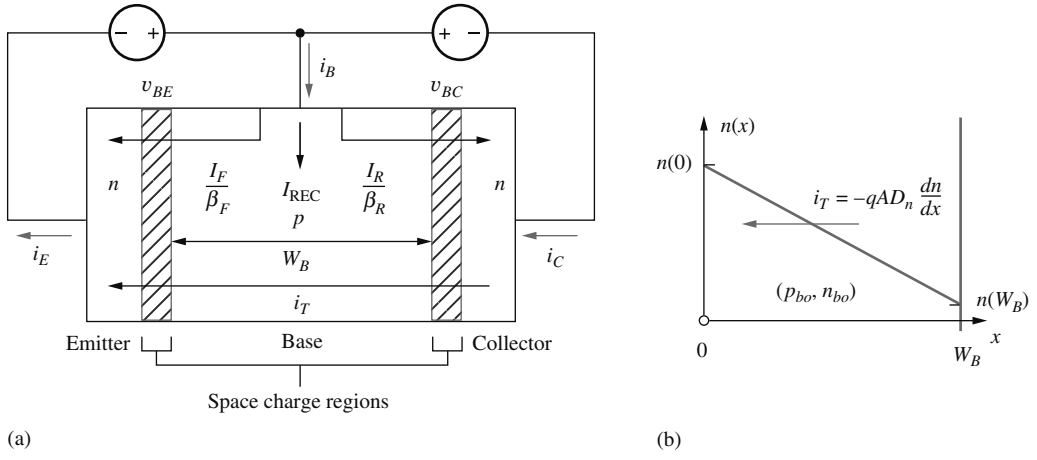


Figure 5.23 (a) Currents in the base region of an *npn* transistor; (b) minority-carrier concentration in the base of the *npn* transistor.

[8] Specially designed power transistors may have breakdown voltages in the 1000-V range.

across the base, and the diffusion current in the base can be calculated using the diffusion current expression in Eq. (2.14):

$$i_T = -qAD_n\frac{dn}{dx} = +qAD_n\frac{n_{bo}}{W_B}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - \exp\left(\frac{v_{BC}}{V_T}\right)\right] \tag{5.31}$$

where A = cross-sectional area of base region and W_B = **base width**. Because the carrier gradient is negative, electron current i_T is directed in the negative x direction, exiting the emitter terminal (positive i_T).

Comparing Eqs. (5.31) and (5.18) yields a value for the bipolar transistor saturation current I_S:

$$I_S = qAD_n\frac{n_{bo}}{W_B} = \frac{qAD_n n_i^2}{N_{AB}W_B} \tag{5.32a}$$

where N_{AB} = doping concentration in base of transistor, n_i = intrinsic-carrier concentration (10^{10}/cm^3), and $n_{bo} = n_i^2/N_{AB}$ using Eq. (2.12).

The corresponding expression for the saturation current of the *pnp* transistor is

$$I_S = qAD_p\frac{p_{bo}}{W_B} = \frac{qAD_p n_i^2}{N_{DB}W_B} \tag{5.32b}$$

Remembering from Chapter 2 that mobility μ, and hence diffusivity $D = (kT/q)\mu$ (cm^2/s), is larger for electrons than holes ($\mu_n > \mu_p$), we see from Eqs. (5.32) that the *npn* transistor will conduct a higher current than the *pnp* transistor for a given set of applied voltages.

EXERCISE: (a) What is the value of D_n at room temperature if $\mu_n = 500$ cm^2/V · s? (b) What is I_S for a transistor with $A = 50$ μm^2, $W = 1$ μm, $D_n = 12.5$ cm^2/s, and $N_{AB} = 10^{18}$/cm^3?

ANSWERS: 12.5 cm^2/s; 10^{-18} A

5.8.3 BASE TRANSIT TIME

To turn on the bipolar transistor, minority-carrier charge must be introduced into the base to establish the carrier gradient in Fig. 5.23(b). The **forward transit time** τ_F represents the time constant associated with storing the required charge Q in the base region and is defined by

$$\tau_F = \frac{Q}{I_T} \tag{5.33}$$

Figure 5.24 depicts the situation in the neutral base region of an *npn* transistor operating in the forward-active region with $v_{BE} > 0$ and $v_{BC} = 0$. The area under the triangle represents the excess minority charge Q that must be stored in the base to support the diffusion current. For the dimensions in Fig. 5.24 and using Eq. (5.30)

$$Q = qA[n(0) - n_{bo}]\frac{W_B}{2} = qAn_{bo}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]\frac{W_B}{2} \tag{5.34}$$

For the conditions in Fig. 5.24(a),

$$i_T = \frac{qAD_n}{W_B}n_{bo}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \tag{5.35}$$

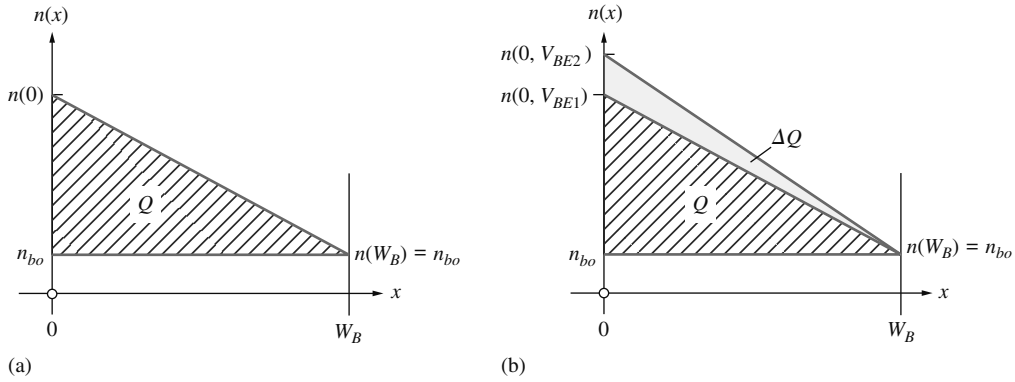


Figure 5.24 (a) Excess minority charge Q stored in the bipolar base region; (b) stored charge Q changes as v_{BE} changes.

Substituting Eqs. (5.34) and (5.35) into Eq. (5.33), the forward transit time for the *npn* transistor is found to be

$$\tau_F = \frac{W_B^2}{2D_n} = \frac{W_B^2}{2V_T\mu_n} \tag{5.36a}$$

The corresponding expression for the transit time of the *pnp* transistor is

$$\tau_F = \frac{W_B^2}{2D_p} = \frac{W_B^2}{2V_T\mu_p} \tag{5.36b}$$

The base transit time can be viewed as the average time required for a carrier emitted by the emitter to arrive at the collector. Hence, one would not expect the transistor to be able to reproduce frequencies with periods that are less than the transit time, and the base transit time in Eq. (5.36) places an upper limit on the useful operating frequency f of the transistor:

$$f \leq \frac{1}{2\pi\tau_F} \tag{5.37}$$

From Eq. (5.36), we see that the transit time is inversely proportional to the minority-carrier mobility in the base, and the difference between electron and hole mobility leads to an inherent frequency and speed advantage for the *npn* transistor. Thus, an *npn* transistor may be expected to be 2 to 2.5 times as fast as a *pnp* transistor for a given geometry and doping. Equation (5.36) also indicates the importance of shrinking the base width W_B of the transistor as much as possible. Early transistors had base widths of 10 μm or more, whereas the base width of transistors in research laboratories today is 0.1 μm (100 nm) or less.

EXAMPLE 5.8 SATURATION CURRENT AND TRANSIT TIME

Device physics has provided us with expressions that can be used to estimate transistor saturation current and transit time based on a knowledge of physical constants and structural device information. Here we find representative values of I_S and τ_F for a bipolar transistor.

PROBLEM Find the saturation current and base transit time for an *npn* transistor with a 100 μm × 100 μm emitter region, a base doping of $10^{17}/\text{cm}^3$, and a base width of 1 μm. Assume $\mu_n = 500\ \text{cm}^2/\text{V}\cdot\text{s}$.

SOLUTION **Known Information and Given Data:** Emitter area = 100 μm × 100 μm, $N_{AB} = 10^{17}/\text{cm}^3$, $W_B = 1$ μm, $\mu_n = 500\ \text{cm}^2/\text{V}\cdot\text{s}$

Unknowns: Saturation current I_S; transit time τ_F

Approach: Evaluate Eqs. (5.33) and (5.37) using the given data.

Assumptions: Room temperature operation with $V_T = 0.025$ V and $n_i = 10^{10}/\text{cm}^3$

Analysis: Using Eq. (5.32) for I_S:

$$I_S = \frac{qAD_n n_i^2}{N_{AB} W_B} = \frac{(1.6 \times 10^{-19}\ \text{C})(10^{-2}\ \text{cm})^2 \left(0.025\ \text{V} \times 500\ \frac{\text{cm}^2}{\text{V} \cdot \text{s}}\right)\left(\frac{10^{20}}{\text{cm}^6}\right)}{\left(\frac{10^{17}}{\text{cm}^3}\right)(10^{-4}\ \text{cm})} = 2 \times 10^{-15}\ \text{A}$$

in which $D_n = (kT/q)\mu_n$ has been used [remember Eq. (2.15)].

Using Eq. (5.36)

$$\tau_F = \frac{W_B^2}{2V_T \mu_n} = \frac{(10^{-4}\ \text{cm})^2}{2(0.025\ \text{V})\left(500\ \frac{\text{cm}^2}{\text{V} \cdot \text{s}}\right)} = 4 \times 10^{-10}\ \text{s}$$

Check of Results: The calculations appear correct, and the value of I_S is within the range given in Sec. 5.2.

Discussion: Operation of this particular transistor is limited to frequencies below $f = 1/(2\pi\tau_F) =$ 400 MHz.

5.8.4 DIFFUSION CAPACITANCE

Capacitances are circuit elements that limit the high-frequency performance of both MOS and bipolar devices. For the base-emitter voltage and hence the collector current in the BJT to change, the charge stored in the base region also must change, as illustrated in Fig. 5.24(b). This change in charge with v_{BE} can be modeled by a capacitance $\boldsymbol{C_D}$, called the **diffusion capacitance,** placed in parallel with the forward-biased base-emitter diode as defined by

$$C_D = \left.\frac{dQ}{dv_{BE}}\right|_{\text{Q-point}} = \frac{1}{V_T}\frac{qAn_{bo}W_B}{2}\exp\left(\frac{V_{BE}}{V_T}\right) \tag{5.38}$$

This equation can be rewritten as

$$C_D = \frac{1}{V_T}\left[\frac{qAD_n n_{bo}}{W_B}\exp\left(\frac{V_{BE}}{V_T}\right)\right]\left(\frac{W_B^2}{2D_n}\right) \cong \frac{I_T}{V_T}\tau_F \tag{5.39}$$

Because the transport current actually represents the collector current in the forward-active region, the expression for the diffusion capacitance is normally written as

$$C_D = \frac{I_C}{V_T}\tau_F \tag{5.40}$$

From Eq. (5.40), we see that the diffusion capacitance C_D is directly proportional to current and inversely proportional to temperature T. For example, a BJT operating at a current of 1 mA with $\tau_F = 4 \times 10^{-10}$ s has a diffusion capacitance of

$$C_D = \frac{I_C}{V_T}\tau_F = \frac{10^{-3}\ \text{A}}{0.025\ \text{V}}\left(4 \times 10^{-10}\ \text{s}\right) = 16 \times 10^{-12}\ \text{F} = 16\ \text{pF}$$

This is a substantial capacitance, but it can be even larger if the transistor is operating at significantly higher currents.

EXERCISE: Calculate the value of the diffusion capacitance for a power transistor operating at a current of 10 A and a temperature of 100°C if $\tau_F = 4$ nS.

ANSWER: 1.24 μF — a significant capacitance!

5.8.5 FREQUENCY DEPENDENCE OF THE COMMON-EMITTER CURRENT GAIN

The forward-biased diffusion and reverse-biased *pn* junction capacitances of the bipolar transistor cause the current gain of the transistor to be frequency-dependent. An example of this dependence is given in Fig. 5.25. At low frequencies, the current gain has a constant value β_F, but as frequency increases, the current gain begins to decrease. The **unity-gain frequency** f_T is defined to be the frequency at which the magnitude of the current gain is equal to 1. The behavior in the graph is described mathematically by

$$\beta(f) = \frac{\beta_F}{\sqrt{1 + \left(\frac{f}{f_\beta}\right)^2}} \tag{5.41}$$

where $f_\beta = f_T/\beta_F$ is the **β-cutoff frequency.** For the transistor in Fig. 5.25, $\beta_F = 125$ and $f_T = 300$ MHz.

EXERCISE: What is the β-cutoff frequency for the transistor in Fig. 5.25?

ANSWER: 2.4 MHz

5.8.6 THE EARLY EFFECT AND EARLY VOLTAGE

In the transistor output characteristics in Fig. 5.10, the current is saturated at a constant value in the forward-active region. However, in a real transistor, there is actually a positive slope to the characteristics, as shown in Fig. 5.26. The collector current is not truly independent of v_{CE}. Note that this situation is the same as that found for the MOSFET in saturation.

It has been observed experimentally that when the output characteristic curves are extrapolated back to the point of zero collector current, the curves all intersect at approximately a common

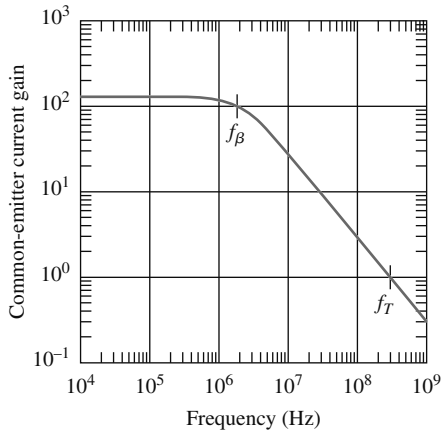


Figure 5.25 Magnitude of the common-emitter current gain β vs. frequency.

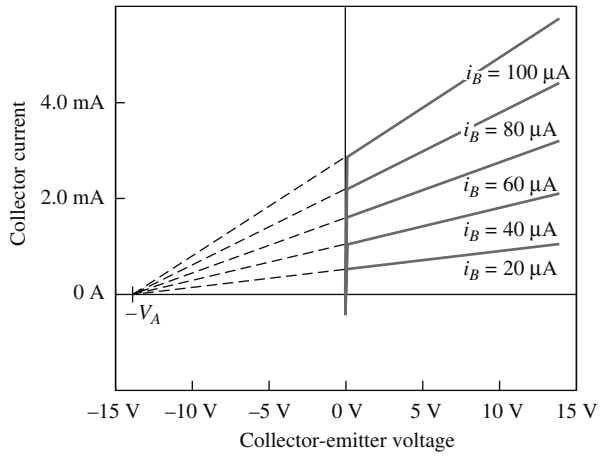


Figure 5.26 Transistor output characteristics identifying the Early voltage V_A.

point, $v_{CE} = -V_A$. This phenomenon is called the **Early effect** [7], and the voltage V_A is called the **Early voltage** after James Early from Bell Laboratories, who first identified the source of the behavior. A relatively small value of Early voltage (14 V) has been used in Fig. 5.26 to exaggerate the characteristics. Values for the Early voltage more typically fall in the range

$$10\ \text{V} \leq V_A \leq 200\ \text{V}$$

5.8.7 MODELING THE EARLY EFFECT

The dependence of the collector current on collector-emitter voltage is easily included in the simplified mathematical model for the forward-active region of the BJT by modifying Eqs. (5.23) as follows:

$$\begin{aligned} i_C &= I_S \left[\exp\left(\frac{v_{BE}}{V_T}\right)\right]\left[1 + \frac{v_{CE}}{V_A}\right] \\ \beta_F &= \beta_{FO}\left[1 + \frac{v_{CE}}{V_A}\right] \\ i_B &= \frac{I_S}{\beta_{FO}}\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right] \end{aligned} \tag{5.42}$$

β_{FO} represents the value of β_F extrapolated to $V_{CE} = 0$. In these expressions, the collector current and current gain now have the same dependence on v_{CE}, but the base current remains independent of v_{CE}. This result assumes that the current gain is determined by back injection into the emitter [9]. This is consistent with Fig. 5.26, in which the separation of the constant-base-current curves in the forward-active region increases as v_{CE} increases, indicating that the current gain β_F is increasing with v_{CE}.

EXERCISE: A transistor has $I_S = 10^{-15}$ A, $\beta_{FO} = 75$, and $V_A = 50$ V and is operating with $V_{BE} = 0.7$ V and $V_{CE} = 10$ V. What are I_B, β_F, and I_C? What would be β_F and I_C if $V_A = \infty$?

ANSWERS: 19.3 μA, 90, 1.74 mA; 75, 1.45 mA

5.8.8 ORIGIN OF THE EARLY EFFECT

Modulation of the base width W_B of the transistor by the collector-base voltage is the cause of the Early effect. As the reverse bias across the collector-base junction increases, the width of the collector-base depletion layer increases, and width W_B of the base decreases. This mechanism, termed **base-width modulation,** is depicted in Fig. 5.27, in which the collector-base space charge region

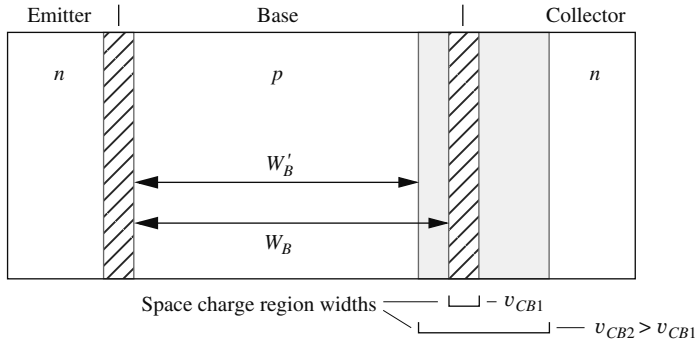


Figure 5.27 Base-width modulation, or Early effect.

width is shown for two different values of collector-base voltage corresponding to effective base widths of W_B and W_B'. Equation (5.31) demonstrated that collector current is inversely proportional to the base width W_B, so a decrease in W_B results in an increase in transport current i_T. This decrease in W_B as V_{CB} increases is the cause of the Early effect.

The Early effect reduces the output resistance of the bipolar transistor and places an important limit on the amplification factor of the BJT. These limitations are discussed in detail in Part III, Chapter 13. Note that both the Early effect in the BJT and channel-length modulation in the MOSFET are similar in the sense that the nonzero slope of the output characteristics is related to changes in a characteristic length within the device as the voltage across the output terminals of the transistor changes.

5.9 TRANSCONDUCTANCE

The important transistor parameter, **transconductance** g_m, was introduced during our study of the MOSFET in Chapter 4. For the bipolar transistor, g_m relates changes in i_C to changes in v_{BE} as defined by

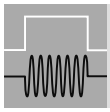
$$g_m = \left.\frac{di_C}{dv_{BE}}\right|_{\text{Q-point}} \tag{5.43}$$

For Q-points in the forward-active region, Eq. (5.43) can be evaluated using the collector-current expression from Eq. (5.23):

$$g_m = \left.\frac{d}{dv_{BE}}\left\{I_S \exp\left(\frac{v_{BE}}{V_T}\right)\right\}\right|_{\text{Q-point}} = \frac{1}{V_T} I_S \exp\left(\frac{V_{BE}}{V_T}\right) = \frac{I_C}{V_T} \tag{5.44}$$

Equation (5.44) represents the fundamental relationship for the transconductance of the bipolar transistor, in which we find g_m is directly proportional to collector current. This is an important result that is used many times in bipolar circuit design. It is worth noting that the expression for the transit time defined in Eq. (5.40) can be rewritten as

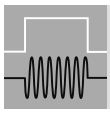
$$\tau_F = \frac{C_D}{g_m} \qquad \text{or} \qquad C_D = g_m \tau_F \tag{5.45}$$



DESIGN NOTE **BIPOLAR TRANSCONDUCTANCE**

$$g_m = \frac{I_C}{V_T}$$

The BJT transconductance is substantially higher than that of the FET for a given operating current. This difference will be discussed in more detail in Chapters 13 and 14.



DESIGN NOTE **TRANSIT TIME**

$$\tau_F = \frac{C_D}{g_m}$$

Transit time τ_F places an upper limit on the frequency response of the bipolar device.

EXERCISE: What is the value of the BJT transconductance g_m at $I_C = 100$ μA and $I_C = 1$ mA? What is the value of the diffusion capacitance for each of these currents if the base transit time is 25 ps?

ANSWERS: 4 mS; 40 mS; 0.1 pF; 1.0 pF

5.10 BIPOLAR TECHNOLOGY AND SPICE MODEL

In order to create a comprehensive simulation model of the bipolar transistor, our knowledge of the physical structure of the transistor is coupled with the transport model expressions and experimental observations. We typically start with a circuit representation of our mathematical model that describes the intrinsic behavior of the transistor, and then add additional elements to model parasitic effects introduced by the actual physical structure. Remember, in any case, that our SPICE models represent only lumped element equivalent circuits for the distributed structure that we actually fabricate.

Although we will seldom use the equations that make up the simulation model in hand calculations, awareness and understanding of the equations can help when SPICE generates unexpected results. This can happen when we attempt to use a device in an unusual way, or the simulator may produce a circuit result that does not fit within our understanding of the device behavior. Understanding the internal model is SPICE will help us interpret whether our knowledge of the device is wrong or if the simulation has some built-in assumptions that may not be consistent with a particular application of the device.

5.10.1 QUALITATIVE DESCRIPTION

A detailed cross section of the classic *npn* structure from Fig. 5.1 is given in Fig. 5.28(a), and the corresponding SPICE circuit model appears in Fig. 5.28(b). Circuit elements i_C, i_B, C_{BE}, and C_{BC} describe the intrinsic transistor behavior that we have discussed thus far. Current source i_C represents the current transported across the base from collector to emitter, and current source i_B models the total base current of the transistor. **Base-emitter** and **base-collector** capacitances C_{BE} and C_{BC} include

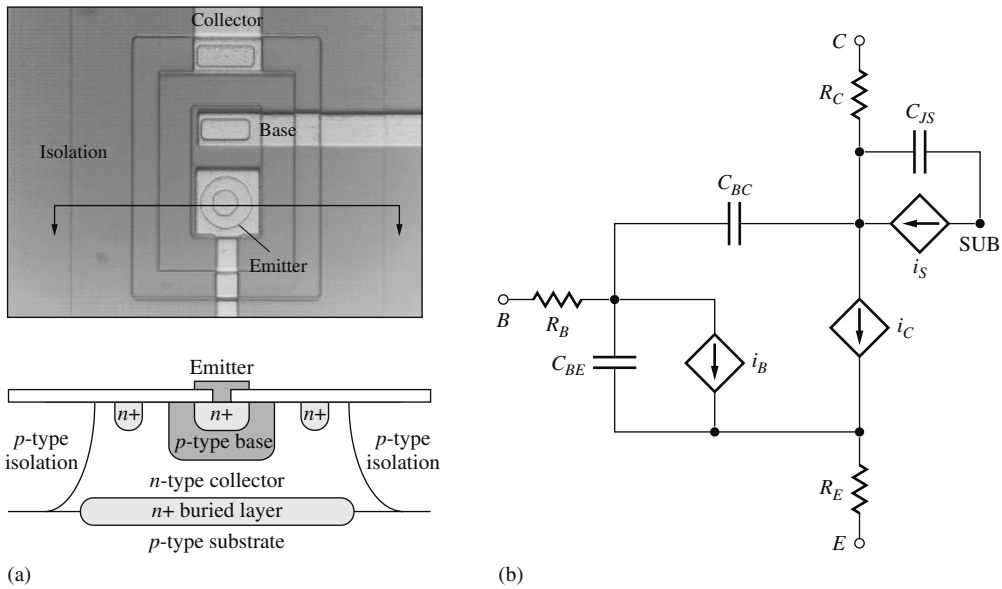


Figure 5.28 (a) Top view and cross section of a junction-isolated transistor; (b) SPICE model for the *npn* transistor.

models for the diffusion capacitances and the junction capacitances associated with the base-emitter and base-collector diodes.

Additional circuit elements are added to account for nonideal characteristics of the real transistor. The physical structure has a large-area *pn* junction that isolates the collector from the substrate of the transistor and separates one transistor from the next. The primary components related to this junction are diode current i_S and capacitance C_{JS}. Base resistance R_B accounts for the resistance between the external base contact and the intrinsic base region of the transistor. Similarly, collector current must pass through R_C on its way to the active region of the collector-base junction, and R_E models any extrinsic emitter resistance present in the device.

5.10.2 SPICE MODEL EQUATIONS

The SPICE models are comprehensive but quite complex. Even the model equations presented below represent simplified versions of the actual models. Table 5.3 defines the SPICE parameters that are used in these expressions. More complete descriptions can be found in [8].

The collector and base currents are given by

$$i_C = \frac{(i_F - i_R)}{\text{KBQ}} - \frac{i_R}{\text{BR}} - i_{RG} \qquad \text{and} \qquad i_B = \frac{i_F}{\text{BF}} + \frac{i_R}{\text{BR}} + i_{FG} + i_{RG}$$

TABLE 5.3
Bipolar Device Parameters for Circuit Simulation (*npn*/ *pnp*)

PARAMETER	NAME	DEFAULT	TYPICAL VALUES
Saturation current	**IS**	10^{-16} A	3×10^{-17} A
Forward current gain	**BF**	100	100
Forward emission coefficient	NF	1	1.03
Forward Early voltage	**VAF**	∞	75 V
Forward knee current	IKF	∞	0.05 A
Reverse knee current	IKR	∞	0.01 A
Reverse current gain	BR	1	0.5
Reverse emission coefficient	NR	1	1.05
Base resistance	RB	0	250 Ω
Collector resistance	RC	0	50 Ω
Emitter resistance	RE	0	1 Ω
Forward transit time	TF	0	0.15 ns
Reverse transit time	TR	0	15 ns
Base-emitter leakage saturation current	ISE	0	1 pA
Base-emitter leakage emission coefficient	NE	1.5	1.4
Base-emitter junction capacitance	CJE	0	0.5 pF
Base-emitter junction potential	PHIE	0.8 V	0.8 V
Base-emitter grading coefficient	ME	0.5	0.5
Base-collector leakage saturation current	ISC	0	1 pA
Base-collector leakage emission coefficient	NC	1.5	1.4
Base-collector junction capacitance	CJC	0	1 pF
Base-collector junction potential	PHIC	0.75 V	0.7 V
Base-collector grading coefficient	MC	0.33	0.33
Substrate saturation current	ISS	0	1 fA
Substrate emission coefficient	NS	1	1
Collector-substrate junction capacitance	CJS	0	3 pF
Collector-substrate junction potential	VJS	0.75 V	0.75 V
Collector-substrate grading coefficient	MJS	0	0.5

in which the forward and reverse components of the transport current are

$$i_F = \text{IS} \cdot \left[\exp\left(\frac{v_{BE}}{\text{NF} \cdot V_T}\right) - 1\right] \qquad \text{and} \qquad i_R = \text{IS} \cdot \left[\exp\left(\frac{v_{BC}}{\text{NR} \cdot V_T}\right) - 1\right] \tag{5.46}$$

Base current i_B includes two added terms to model additional space-charge region currents associated with the base-emitter and base-collector junctions:

$$i_{FG} = \text{ISE} \cdot \left[\exp\left(\frac{v_{BE}}{\text{NE} \cdot V_T}\right) - 1\right] \qquad \text{and} \qquad i_{RG} = \text{ISC} \cdot \left[\exp\left(\frac{v_{BC}}{\text{NC} \cdot V_T}\right) - 1\right]$$

Another new addition is the KBQ term that includes voltages VAF and VAR to model the Early effect in both the forward and reverse modes, as well as "knee current" parameters IKF and IKR that model current gain fall-off at high operating currents. This phenomenon is discussed in more detail in Chapter 13.

$$\text{KBQ} = \left(\frac{1}{2}\right) \frac{1 + \left[1 + 4\left(\dfrac{i_F}{\text{IKF}} + \dfrac{i_R}{\text{IKR}}\right)\right]^{NK}}{1 + \dfrac{v_{CB}}{\text{VAF}} + \dfrac{v_{EB}}{\text{VAR}}}$$

Note as well that the Early effect is cast in terms of v_{BC} rather than v_{CE} as we have used in Eq. (5.42).

The substrate junction current is expressed as

$$i_S = \text{ISS} \cdot \left[\exp\left(\frac{v_{\text{SUB-C}}}{\text{NS} \cdot V_T}\right) - 1\right]$$

The three device capacitances in Fig. 5.28(b) are represented by

$$C_{BE} = \frac{i_F}{\text{NE} \cdot V_T}\text{TF} + \frac{\text{CJE}}{\left(1 - \dfrac{v_{BE}}{\text{PHIE}}\right)^{\text{MJE}}} \qquad \text{and} \qquad C_{BC} = \frac{i_R}{\text{NC} \cdot V_T}\text{TR} + \frac{\text{CJC}}{\left(1 - \dfrac{v_{BC}}{\text{PHIC}}\right)^{\text{MJC}}}$$

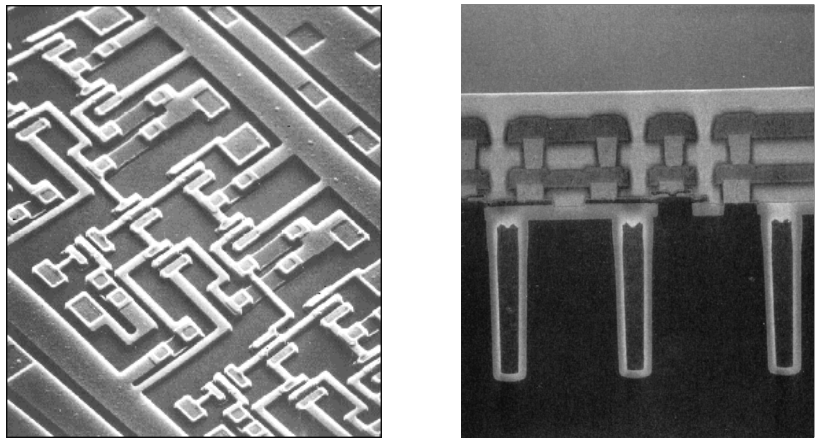
$$C_{JS} = \frac{\text{CJS}}{\left(1 + \dfrac{v_{\text{SUB-C}}}{\text{VJS}}\right)^{\text{MJS}}} \tag{5.47}$$

C_{BE} and C_{BC} consist of two terms representing the diffusion capacitance (modeled by TF and NE or TR and NC) and depletion-region capacitance (modeled by CJE, PHIE, and MJE or CJC, PHIC, and MJC). The substrate diode is normally reverse biased, so it is modeled by just the depletion-layer capacitance (CJS, VJS, and MJS). The base, collector, and emitter series resistances are RB, RC, and RE, respectively.

The SPICE model for the *pnp* transistor is similar to that presented in Fig. 5.28(b) except for reversal of the current sources and of the positive polarity for the transistor currents and voltages.

5.10.3 HIGH-PERFORMANCE BIPOLAR TRANSISTORS

Modern transistors designed for high-speed switching and analog RF applications use combinations of sophisticated shallow and deep trench isolation processes to reduce the device capacitances and minimize the transit times. These devices typically utilize polysilicon emitters, have extremely narrow bases, and may incorporate SiGe base regions. A layout and cross section of a very high frequency, trench-isolated SiGe bipolar transistor appear in Fig. 5.29. In the research laboratory, SiGe transistors have already exhibited cutoff frequencies in excess of 300 GHz.



(a) (b)

Figure 5.29 (a) Top view of a high-performance trench-isolated integrated circuit; (b) cross section of a high-performance trench-isolated bipolar transistor. J.D. Cressler, "Reengineering silicon: SiGe heterojunction bipolar technology," *IEEE Spectrum*, Vol. 32, Issue: 3, pp. 49–55. March 1995. *Copyright ©1995, IEEE. Reprinted with permission.*

EXERCISE: A bipolar transistor has a current gain of 80, a collector current of 350 μA for $V_{BE} =$ 0.68 V, and an Early voltage of 70 V. What are the values of SPICE parameters BF, IS, and VAF? Assume $T = 27^{\circ}$C.

ANSWERS: 80, 1.39 fA, 70 V

5.11 PRACTICAL BIAS CIRCUITS FOR THE BJT

The goal of biasing is to establish a known **quiescent operating point,** or **Q-point** that represents the initial operating region of the transistor. In the bipolar transistor, the Q-point is represented by the dc values of the collector-current and collector-emitter voltage (I_C, V_{CE}) for the *npn* transistor, or emitter-collector voltage (I_C, V_{EC}) for the *pnp*.

Logic gates and linear amplifiers use very different operating points. For example, the circuit in Fig. 5.30(a) can be used as either a logic inverter or a linear amplifier depending upon our choice of operating points. The voltage transfer characteristic (VTC) for the circuit appears in Fig. 5.31(a), and the corresponding output characteristics and load line appear in Fig. 5.31(b). For low values of v_{BE}, the transistor is nearly cut off, and the output voltage is 5 V, corresponding to a binary "1" in a logic applications. As v_{BE} increases above 0.6 V, the output drops quickly and reaches its "on-state" voltage of 0.18 V for v_{BE} greater than 0.8 V. The BJT is now operating in its saturation region, and the small "on-voltage" would correspond to a "0" in binary logic. These two logic states are also shown on the transistor output characteristics in Fig. 5.31(b). When the transistor is "on," it conducts a substantial current, and v_{CE} falls to 0.18 V. When the transistor is off, v_{CE} equals 5 V. We study the design of logic gates in detail in Chapters 6 – 9.

For amplifier applications, the Q-point is located in the region of high slope (high gain) of the voltage transfer characteristic, also indicated in Fig. 5.31(a). At this operating point, the transistor is operating in the forward-active region, the region in which high voltage, current, and/or power gain can be achieved. To establish this Q-point, a **dc bias** V_{BE} is applied to the base as in Fig. 5.30(b), and a small ac signal v_{be} is added to vary the base voltage around the bias value.[9] The variation in

[9] Remember $v_{BE} = V_{BE} + v_{be}$.

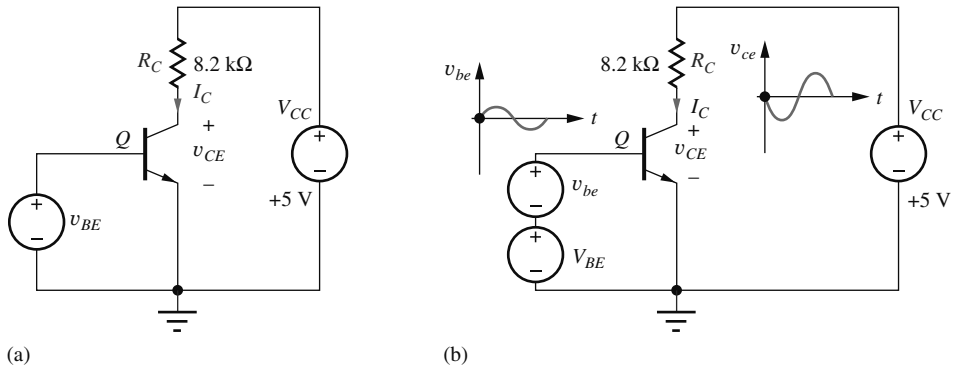


Figure 5.30 (a) Circuit for a logic inverter; (b) the same transistor used as a linear amplifier.

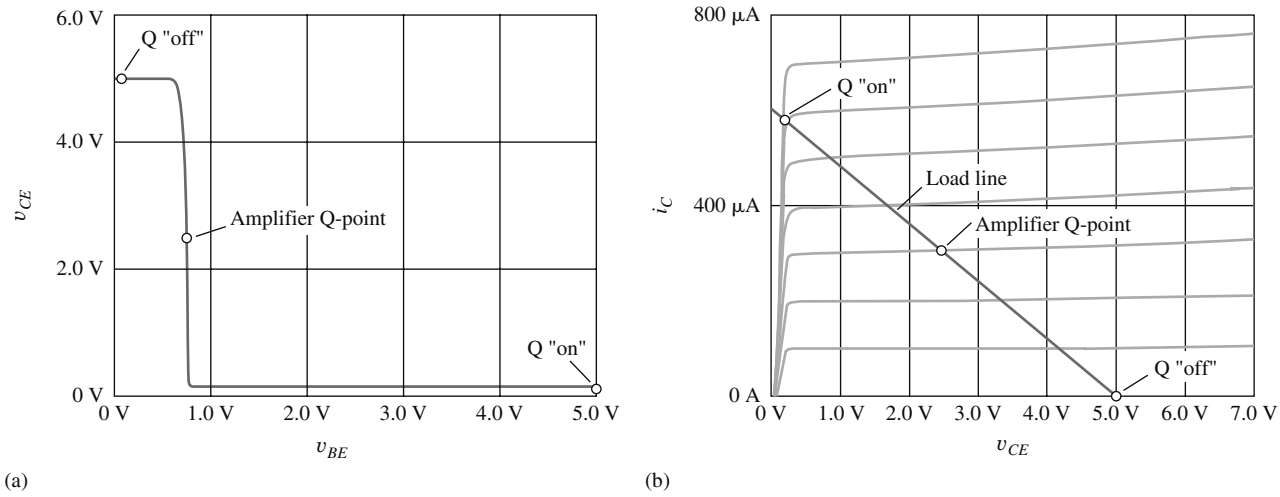


Figure 5.31 (a) Voltage transfer characteristic (VTC) with quiescent operating points (Q-points) corresponding to an "on-switch," an amplifier, and an "off switch"; (b) the same three operating points located on the transistor output characteristics.

total base-emitter voltage v_{BE} causes the collector current to change, and an amplified replica of the ac input voltage appears at the collector. Our study of the design of transistor amplifiers begins in Chapter 13 of this book.

In Secs. 5.6 to 5.10, we presented simplified models for the four operating regions of the BJT. In general, we will not explicitly insert the simplified circuit models for the transistor into the circuit but instead will use the mathematical relationships that were derived for the specific operating region of interest. For example, in the forward-active region, the results $V_{BE} = 0.7$ V and $I_C = \beta_F I_B$ will be utilized to directly simplify the circuit analysis.

In the dc biasing examples that follow, the Early voltage is assumed to be infinite. In general, including the Early voltage in bias circuit calculations substantially increases the complexity of the analysis but typically changes the results by less than 10 percent. In most cases, the tolerances on the values of resistors and independent sources will be 5 to 10 percent, and the transistor current-gain β_F may vary by a factor of 4:1 to 10:1. For example, the current gain of a transistor may be specified to be a minimum of 50 with a typical value of 100 but no upper bound specified. These tolerances will swamp out any error due to neglect of the Early voltage. Thus, basic hand design will be done ignoring the Early effect, and if more precision is needed, the calculations can be refined through SPICE analysis.

5.11.1 FOUR-RESISTOR BIAS NETWORK

Because of the BJT's exponential relationship between current and voltage and its strong dependence on temperature T, the constant V_{BE} form of biasing utilized in Fig. 5.30 does not represent a practical technique. One of the best circuits for stabilizing the Q-point of a transistor is the four-resistor bias network in Fig. 5.32. R_1 and R_2 form a resistive voltage divider across the power supplies (12 V and 0 V) and attempt to establish a fixed voltage at the base of transistor Q_1. R_E and R_C are used to define the emitter current and collector-emitter voltage of the transistor.

Our goal is to find the Q-point of the transistor: (I_C, V_{CE}). The first steps in analysis of the circuit in Fig. 5.32(a) are to split the power supply into two equal voltages, as in Fig. 5.32(b), and then to simplify the circuit by replacing the base-bias network by its Thévenin equivalent circuit, as shown in Fig. 5.32(c). V_{EQ} and R_{EQ} are given by

$$V_{EQ} = V_{CC}\frac{R_1}{R_1 + R_2} \qquad R_{EQ} = \frac{R_1 R_2}{R_1 + R_2} \tag{5.48}$$

For the values in Fig. 5.32(c), $V_{EQ} = 4$ V and $R_{EQ} = 12$ kΩ.

Detailed analysis begins by assuming a region of operation in order to simplify the BJT model equations. Because the most common region of operation for this bias circuit is the forward-active

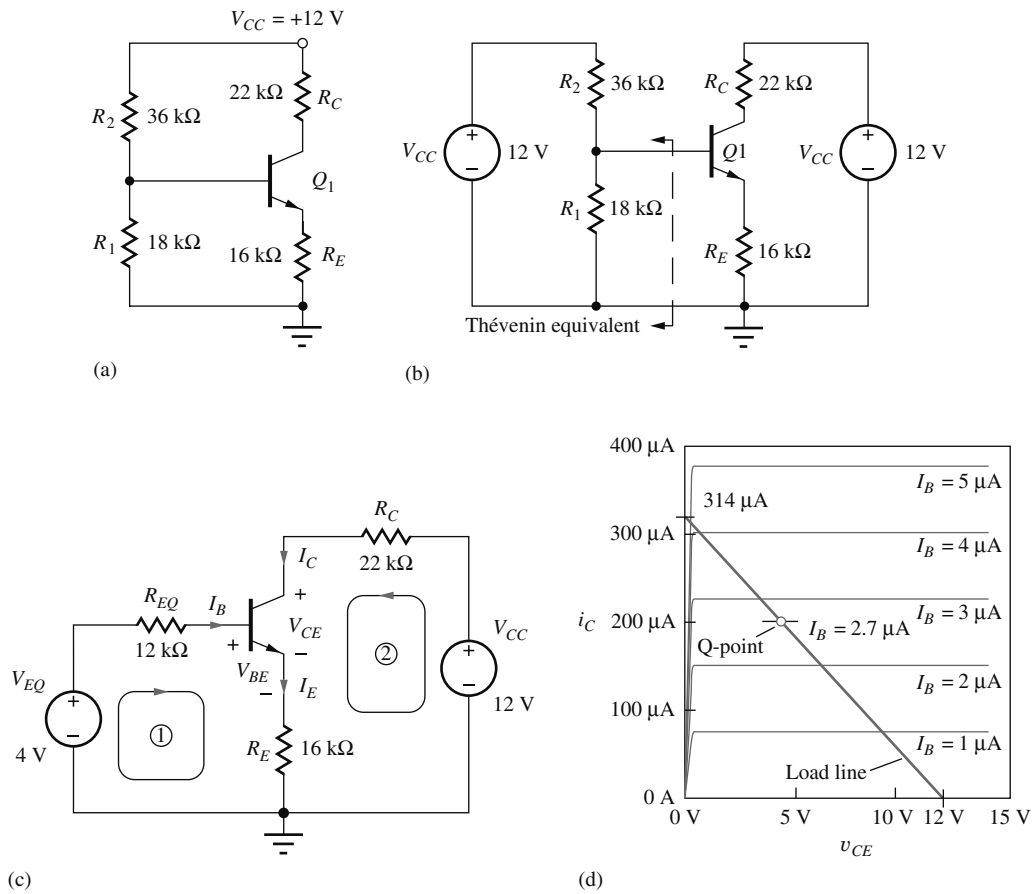


Figure 5.32 (a) The four-resistor bias network (assume $\beta_F = 75$ for analysis); (b) four-resistor bias circuit with replicated sources; (c) Thévenin simplification of the four-resistor bias network (assume $\beta_F = 75$); (d) load line for the four-resistor bias circuit.

region, we will assume it to be the region of operation. Using Kirchhoff's voltage law around loop 1:

$$V_{EQ} = I_B R_{EQ} + V_{BE} + I_E R_E = I_B R_{EQ} + V_{BE} + (\beta_F + 1) I_B R_E \tag{5.49}$$

Solving for I_B yields

$$I_B = \frac{V_{EQ} - V_{BE}}{R_{EQ} + (\beta_F + 1) R_E} \quad \text{where} \quad V_{BE} = V_T \ln\left(\frac{I_B}{I_S/\beta_F} + 1\right) \tag{5.50}$$

Unfortunately, combining these expressions yields a transcendental equation. However, if we assume an approximate value of V_{BE}, then we can find the collector and emitter currents using our auxillary relationships $I_C = \beta_F I_B$ and $I_E = (\beta_F + 1) I_B$:

$$I_C = \frac{V_{EQ} - V_{BE}}{\dfrac{R_{EQ}}{\beta_F} + \dfrac{(\beta_F + 1)}{\beta_F} R_E} \quad \text{and} \quad I_E = \frac{V_{EQ} - V_{BE}}{\dfrac{R_{EQ}}{(\beta_F + 1)} + R_E} \tag{5.51}$$

For large current gain ($\beta_F \gg 1$), Eqs. (5.50) and (5.51) simplify to

$$I_E \cong I_C \cong \frac{V_{EQ} - V_{BE}}{\dfrac{R_{EQ}}{\beta_F} + R_E} \quad \text{with} \quad I_B \cong \frac{V_{EQ} - V_{BE}}{R_{EQ} + \beta_F R_E} \tag{5.52}$$

Now that I_C is known, we can use loop 2 to find collector-emitter voltage V_{CE}:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = V_{CC} - I_C\left(R_C + \frac{R_E}{\alpha_F}\right) \tag{5.53}$$

since $I_E = I_C/\alpha_F$. Normally $\alpha_F \cong 1$, and Eq. (5.53) can be simplified to

$$V_{CE} \cong V_{CC} - I_C(R_C + R_E) \tag{5.54}$$

For the circuit in Fig. 5.32, we are assuming forward-active region operation with $V_{BE} = 0.7$ V, and the Q-point values (I_C, V_{CE}) are

$$I_C \cong \frac{V_{EQ} - V_{BE}}{\dfrac{R_{EQ}}{\beta_F} + R_E} = \frac{(4 - 0.7)\text{V}}{\dfrac{12\,\text{k}\Omega}{75} + 16\,\text{k}\Omega} = 204\,\mu\text{A} \quad \text{with} \quad I_B = \frac{204\,\mu\text{A}}{75} = 2.72\,\mu\text{A}$$

$$V_{CE} \cong V_{CC} - I_C(R_C + R_E) = 12 - 2.04\,\mu\text{A}(22\,\text{k}\Omega + 16\,\text{k}\Omega) = 4.25\,\text{V}$$

A more precise estimate using Eqs. (5.51) and (5.53) gives a Q-point of (202 μA, 4.30 V). Since we don't know the actual value of V_{BE}, and haven't considered any tolerances, the approximate expressions give excellent engineering results.

All the calculated currents are greater than zero, and using the result in Eq. (5.53), $V_{BC} = V_{BE} - V_{CE} = 0.7 - 4.32 = -3.62$ V. Thus, the base-collector junction is reverse-biased, and the assumption of forward-active region operation was correct. The Q-point resulting from our analysis is (204 μA, 4.25 V).

Before leaving this bias example, let us draw the load line for the circuit and locate the Q-point on the output characteristics. The load-line equation for this circuit already appeared as Eq. (5.51):

$$V_{CE} = V_{CC} - \left(R_C + \frac{R_E}{\alpha_F}\right) I_C = 12 - 38{,}200 I_C \tag{5.55}$$

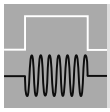
Two points are needed to plot the load line. Choosing $I_C = 0$ yields $V_{CE} = 12$ V, and picking $V_{CE} = 0$ yields $I_C = 314$ μA. The resulting load line is plotted on the transistor common-emitter output characteristics in Fig. 5.32(d). The base current was already found to be 2.7 μA, and the intersection of the $I_B = 2.7$-μA characteristic with the load line defines the Q-point. In this case we must estimate the location of the $I_B = 2.7$-μA curve.

EXERCISE: Find the values of I_B, I_C, I_E, and V_{CE} using the exact expressions in Eqs. (5.50), (5.51), and (5.53).

ANSWERS: 2.69 μA, 202 μA, 204 μA, 4.28 V

EXERCISE: Find the Q-point for the circuit in Fig. 5.32(d) if $R_1 = 180$ kΩ and $R_2 = 360$ kΩ.

ANSWER: (185 μA, 4.93 V)



DESIGN NOTE

Good engineering approximations for the Q-point in the four-resistor bias circuit for the bipolar transistor are:

$$I_C \cong \frac{V_{EQ} - V_{BE}}{\frac{R_{EQ}}{\beta_F} + R_E} \cong \frac{V_{EQ} - V_{BE}}{R_E} \quad \text{and} \quad V_{CE} \cong V_{CC} - I_C(R_C + R_E)$$

5.11.2 DESIGN OBJECTIVES FOR THE FOUR-RESISTOR BIAS NETWORK

Now that we have analyzed a circuit involving the four-resistor bias network, let us explore the design objectives of this bias technique through further simplification of the expression for the collector and emitter currents in Eq. (5.52) by assuming that $R_{EQ}/\beta_F \ll R_E$. Then

$$I_E \cong I_C \cong \frac{V_{EQ} - V_{BE}}{R_E} \tag{5.56}$$

The value of the Thévenin equivalent resistance R_{EQ} is normally designed to be small enough to neglect the voltage drop caused by the base current flowing through R_{EQ}. Under these conditions, I_C and I_E are set by the combination of V_{EQ}, V_{BE}, and R_E. In addition, V_{EQ} is normally designed to be large enough that small variations in the assumed value of V_{BE} will not materially affect the value of I_E.

In the original bias circuit reproduced in Fig. 5.33, the assumption that the voltage drop $I_B R_{EQ} \ll (V_{EQ} - V_{BE})$ is equivalent to assuming $I_B \ll I_2$ so that $I_1 \cong I_2$. For this case, the base current of Q_1 does not disturb the voltage divider action of R_1 and R_2. Using the approximate expression in Eq. (5.54) estimates the emitter current in the circuit in Fig. 5.32 to be

$$I_C \cong I_E \cong \frac{4\text{ V} - 0.7\text{ V}}{16{,}000\ \Omega} = 206\ \mu\text{A}$$

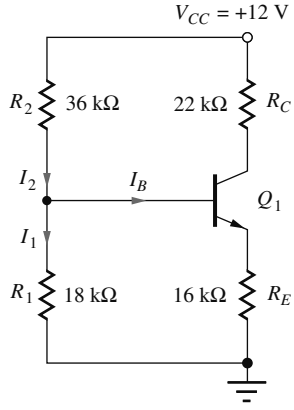


Figure 5.33 Currents in the base-bias network.

which is essentially the same as the result that was calculated using the more exact expression. This is the result that should be achieved with a proper bias network design. If the Q-point is independent of I_B, it will also be independent of current gain β (a poorly controlled transistor parameter). The emitter current will then be approximately the same for a transistor with a current gain of 50 or 500.

Generally, a very large number of possible combinations of R_1 and R_2 will yield the desired value of V_{EQ}. An additional constraint is needed to finalize the design choice. A useful choice is to limit the current used in the base-voltage-divider network by choosing $I_2 \leq I_C/5$. This choice ensures that the power dissipated in bias resistors R_1 and R_2 is less than 20 percent of the total quiescent power consumed by the circuit and at the same time ensures that $I_2 \gg I_B$ for $\beta \geq 50$.

EXERCISE: Show that choosing $I_2 = I_C/5$ is equivalent to setting $I_2 = 10I_B$ when $\beta_F = 50$.

EXERCISE: Find the Q-point for the circuit in Fig. 5.32(a) if β_F is 500.

ANSWER: (206 μA, 4.18 V)

DESIGN EXAMPLE 5.9 FOUR-RESISTOR BIAS DESIGN

Here we explore the design of the network most commonly utilized to bias the BJT — the four-resistor bias circuit.

PROBLEM Design a four resistor bias circuit to give a Q-point of (750 μA, 5 V) using a 15-V supply with an *npn* transistor having a minimum current gain of 100.

SOLUTION **Known Information and Given Data:** The bias circuit in Fig. 5.33 with $V_{CC} = 15$ V; the *npn* transistor has $\beta_F = 100$, $I_C = 750$ μA, and $V_{CE} = 5$ V.

Unknowns: Base voltage V_B, voltages across resistors R_E and R_C; values for R_1, R_2, R_C, and R_E

Approach: First, partition V_{CC} between the collector-emitter voltage of the transistor and the voltage drops across R_C and R_E. Next, choose currents I_1 and I_2 for the base-bias network. Finally, use the assigned voltages and currents to calculate the unknown resistor values.

Assumptions: The transistor is to operate in the forward-active region. The base-emitter voltage of the transistor is 0.7 V. The Early voltage is infinite.

Analysis: To calculate values for the resistors, we must know the voltage across the emitter and collector resistors and the voltage V_B. V_{CE} is designed to be 5 V. One common choice is to divide the remaining power supply voltage $(V_{CC} - V_{CE}) = 10$ V equally between R_E and R_C. Thus, $V_E = 5$ V and $V_C = 5 + V_{CE} = 10$ V. The values of R_C and R_E are then given by

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{5\text{ V}}{750\ \mu\text{A}} = 6.67\ \text{k}\Omega \qquad \text{and} \qquad R_E = \frac{V_E}{I_E} = \frac{5\text{ V}}{758\ \mu\text{A}} = 6.60\ \text{k}\Omega$$

The base voltage is given by $V_B = V_E + V_{BE} = 5.7$ V. For forward-active region operation, we know that $I_B = I_C/\beta_F = 750\ \mu\text{A}/100 = 7.5\ \mu\text{A}$. Now choosing $I_2 = 10I_B$, we have $I_2 = 75\ \mu\text{A}$, $I_1 = 9I_B = 67.5\ \mu\text{A}$, and R_1 and R_2 can be determined:

$$R_1 = \frac{V_B}{9I_B} = \frac{5.7\text{ V}}{67.5\ \mu\text{A}} = 84.4\ \text{k}\Omega \qquad R_2 = \frac{V_{CC} - V_B}{10I_B} = \frac{15 - 5.7\text{ V}}{75\ \mu\text{A}} = 124\ \text{k}\Omega \quad (5.57)$$

Check of Results: We have $V_{BE} = 0.7$ V and $V_{BC} = 5.7 - 10 = -4.3$ V, which are consistent with the forward-active region assumption.

Discussion: The values calculated above should yield a Q-point very close to the design goals. However, if we were going to build this circuit in the laboratory, we must use standard values for the resistors. In order to complete the design, we refer to the table of resistor values in Appendix A. There we find that the closest available values are $R_1 = 82\ \text{k}\Omega$, $R_2 = 120\ \text{k}\Omega$, $R_E = 6.8\ \text{k}\Omega$, and $R_C = 6.8\ \text{k}\Omega$.

Computer-Aided Analysis: SPICE can now be used as a tool to check our design. The final design using these values appears in Fig. 5.34 for which SPICE (with IS $= 2 \times 10^{-15}$ A) predicts the Q-point to be (734 μA, 4.97 V), with $V_{BE} = 0.65$ V. We neglected the Early effect in our hand calculations, but SPICE represents an easy way to check this assumption. If we set VAF = 75 V in SPICE, keeping the other parameters the same, the new Q-point is (737 μA, 4.93 V). Clearly, the changes caused by the Early effect are negligible.

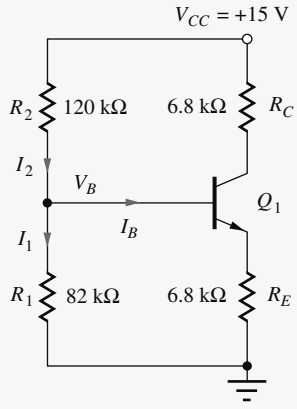
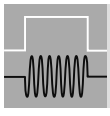


Figure 5.34 Final bias circuit design for a Q-point of (750 μA, 5 V).

EXERCISE: Redesign the four resistor bias circuit to yield $I_C = 75\ \mu\text{A}$ and $V_{CE} = 5$ V.

ANSWERS: (66.7 kΩ, 66.0 kΩ, 844 kΩ, 1.24 MΩ) → (68 kΩ, 68 kΩ, 820 kΩ, 1.20 MΩ)



DESIGN NOTE FOUR-RESISTOR BIAS DESIGN

1. Choose the Thévenin equivalent base voltage V_{EQ}: $\dfrac{V_{CC}}{4} \le V_{EQ} \le \dfrac{V_{CC}}{2}$
2. Select R_1 to set $I_1 = 9I_B$: $R_1 = \dfrac{V_{EQ}}{9I_B}$
3. Select R_2 to set $I_2 = 10I_B$: $R_2 = \dfrac{V_{CC} - V_{EQ}}{10I_B}$
4. R_E is determined by V_{EQ} and the desired collector current: $R_E \cong \dfrac{V_{EQ} - V_{BE}}{I_C}$
5. R_C is determined by the desired collector-emitter voltage: $R_C \cong \dfrac{V_{CC} - V_{CE}}{I_C} - R_E$

EXAMPLE 5.10 TWO-RESISTOR BIASING

In this example, we explore an alternative bias circuit that requires only two resistors and apply it to biasing a *pnp* transistor. (A similar circuit can also be used for *npn* biasing.)

PROBLEM Find the Q-point for the *pnp* transistor in the two-resistor bias circuit in Fig. 5.35. Assume $\beta_F = 50$.

SOLUTION **Known Information and Given Data:** Two-resistor bias circuit in Fig. 5.35 with a *pnp* transistor with $\beta_F = 50$

Unknowns: I_C, V_{CE}

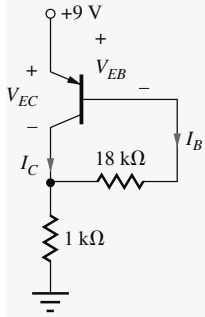


Figure 5.35 Two-resistor bias circuit with a *pnp* transistor.

Approach: Assume a region of operation and analyze the circuit to determine the Q-point; check answer to see if it is consistent with the assumptions.

Assumptions: Forward-active region operation with $V_{EB} = 0.7$ V and $V_A = \infty$

Analysis: The voltages and currents are first carefully labeled as in Fig. 5.35. To find the Q-point, an equation is written involving V_{EB}, I_B, and I_C:

$$9 = V_{EB} + 18{,}000I_B + 1000(I_C + I_B) \tag{5.58}$$

Applying the assumption of forward-active region operation with $\beta_F = 50$ and $V_{EB} = 0.7$ V

$$9 = 0.7 + 18{,}000I_B + 1000(51)I_B \tag{5.59}$$

and

$$I_B = \frac{9\text{ V} - 0.7\text{ V}}{69{,}000\ \Omega} = 120\ \mu\text{A} \qquad I_C = 50I_B = 6.01\text{ mA} \tag{5.60}$$

The emitter-collector voltage is given by

$$V_{EC} = 9 - 1000(I_C + I_B) = 2.88\text{ V} \qquad \text{and} \qquad V_{BC} = 2.18\text{ V} \tag{5.61}$$

The Q-point is $(I_C, V_{EC}) = (6.01\text{ mA}, 2.88\text{ V})$.

Check of Results: Because I_B, I_C, and V_{BC} are all greater than zero, the assumption of forward-active region operation is valid, and the Q-point is correct.

Computer-Aided Analysis: For this circuit, SPICE simulation yields (6.04 mA, 2.95 V), which agrees with the Q-point found from our hand calculations.

EXERCISE: What is the Q-point if the 18-kΩ resistor is increased to 36 kΩ?

ANSWER: (4.77 mA, 4.13 V)

EXERCISE: Draw the two-resistor bias circuit (a "mirror image" of Fig. 5.35) that would be used to bias an *npn* transistor from a single +9-V supply using the same two resistor values as in Fig. 5.35.

ANSWER: See circuit topology in Fig. P5.95.

TABLE 5.4
BJT Iterative Bias Solution $I_S = 10^{-15}\,A$, $V_T = 25$ mV

V_{BE} (V)	I_C (A)	V'_{BE} (V)
0.7000	2.015E−04	0.6507
0.6507	2.046E−04	0.6511
0.6511	2.045E−04	0.6511

The bias circuit examples that have been presented in this section have only scratched the surface of the possible techniques that can be used to bias *npn* and *pnp* transistors. However, the analysis techniques have illustrated the basic approaches that need to be followed in order to determine the Q-point of any bias circuit.

5.11.3 ITERATIVE ANALYSIS OF THE FOUR-RESISTOR BIAS CIRCUIT

To find I_C in the circuit in Fig. 5.32, we need to find a solution to the following pair of equations:

$$I_C = \frac{V_{EQ} - V_{BE}}{\dfrac{R_{EQ}}{\beta_F} + \dfrac{(\beta_F + 1)}{\beta_F} R_E} \quad \text{where} \quad V_{BE} = V_T \ln\left(\frac{I_C}{I_S} + 1\right) \tag{5.62}$$

In the analysis presented in Sec. 5.11, we avoided the problems associated with solving the resulting transcendental equation by assuming that we knew an approximate value for V_{BE}. However, we can find a numerical solution to these two equations with a simple iterative process.

1. Guess a value for V_{BE}.
2. Calculate the corresponding value of I_C using $I_C = \dfrac{V_{EQ} - V_{BE}}{\dfrac{R_{EQ}}{\beta_F} + \dfrac{(\beta_F + 1)}{\beta_F} R_E}$.
3. Update the estimate for V_{BE} as $V'_{BE} = V_T \ln\left(\dfrac{I_C}{I_S} + 1\right)$.
4. Repeat steps 2 and 3 until convergence is obtained.

Table 5.4 presents the results of this iterative method showing convergence in only three iterations. This rapid convergence occurs because of the very steep nature of the $I_C - V_{BE}$ characteristic.

One might ask if this result is better than the one obtained earlier in Sec. 5.11.1. As in most cases, the results are only as good as the input data. Here we need to accurately know the values of saturation current I_S and temperature T in order to calculate V_{BE}. In the earlier solution we simply estimated V_{BE}. In reality, we seldom will know exact values of either I_S or T, so we most often are just satisfied with a direct estimate for V_{BE}.

EXERCISE: Repeat the iterative analysis above to find the values of I_C and V_{BE} if $V_T = 25.8$ mV.

ANSWERS: 203.3 μA, 0.6718 V

5.12 TOLERANCES IN BIAS CIRCUITS

When a circuit is actually built in discrete form in the laboratory or fabricated as an integrated circuit, the components and device parameters all have tolerances associated with their values. Discrete resistors can easily be purchased with 10 percent, 5 percent, or 1 percent tolerances, whereas typical resistors in ICs can exhibit even wider variations (±30 percent). Power supply voltage tolerances are often 5 to 10 percent.

For a given bipolar transistor type, parameters such as current gain may cover a range of 5:1 to 10:1, or may be specified with only a nominal value and lower bound. The BJT (or diode) saturation current may vary by a factor varying from 10:1 to 100:1, and the Early voltage may vary by ±20 percent. In FET circuits, the values of threshold voltage and the transconductance parameter can vary widely, and in op-amp circuits all the op-amp parameters (e.g., open-loop gain, input resistance, output resistance, input bias current, unity gain frequency, and the like) typically exhibit wide specification ranges.

In addition to these initial value uncertainties, the values of the circuit components and parameters change as temperature changes and the circuit ages. It is important to understand the effect of these variations on our circuits and be able to design circuits that will continue to operate correctly in the face of these element variations. Worst-case analysis and Monte Carlo analysis, introduced in Chapter 1, are two approaches that can be used to quantify the effects of tolerances on circuit performance.

5.12.1 WORST-CASE ANALYSIS

Worst-case analysis is often used to ensure that a design will function under an expected set of component variations. In Q-point analysis, for example, the values of components are simultaneously pushed to their various extremes in order to determine the worst possible range of Q-point values. Unfortunately, a design based on worst-case analysis is usually an unnecessary overdesign and economically undesirable, but it is important to understand the technique and its limitations.

EXAMPLE 5.11 WORST-CASE ANALYSIS OF THE FOUR-RESISTOR BIAS NETWORK

Now we explore the application of worst-case analysis to the four-resistor bias network with a given set of tolerances assigned to the elements. In Ex. 5.12, the bounds generated by the worst-case analysis will be compared to a statistical sample of the possible network realizations using Monte Carlo analysis.

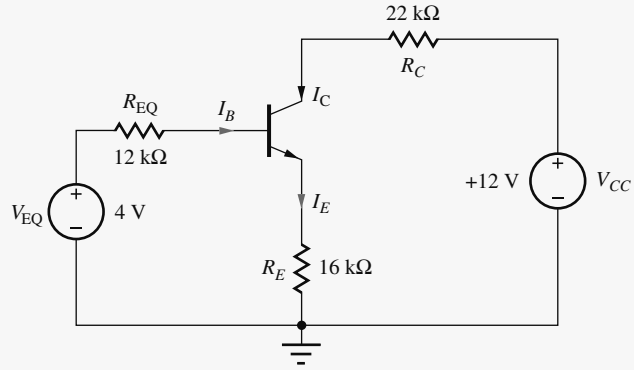


Figure 5.36 Simplified four-resistor bias circuit of Fig. 5.32(c) assuming nominal element values.

PROBLEM Find the worst-case values of I_C and V_{CE} for the transistor circuit in Fig. 5.36 that is the simplified version of the four-resistor bias circuit in Fig. 5.32. Assume that the 12-V power supply has a 5 percent tolerance and the resistors have 10 percent tolerances. Also, assume that the transistor current gain has a nominal value of 75 with a 50 percent tolerance.

SOLUTION **Known Information and Given Data:** Simplified version of the four-resistor bias circuit in Fig. 5.36; 5 percent tolerance on V_{CC}; 10 percent tolerance for each resistor; current $\beta_{FO} = 75$ with a 50 percent tolerance

Unknowns: Minimum and maximum values of I_C and V_{CE}

Approach: Find the worst-case values of V_{EQ} and R_{EQ}; use the results to find the extreme values of the base and collector current; use the collector current values to find the worst-case values of collector-emitter voltage.

Assumptions: To simplify the analysis, assume that the voltage drop in R_{EQ} can be neglected and β_F is large so that I_C is given by

$$I_C \cong I_E = \frac{V_{EQ} - V_{BE}}{R_E} \tag{5.63}$$

Assume V_{BE} is fixed at 0.7 V.

Analysis: To make I_C as large as possible, V_{EQ} should be at its maximum extreme and R_E should be a minimum value. To make I_C as small as possible, V_{EQ} should be minimum and R_E should be a maximum value. Variations in V_{BE} are assumed to be negligible but could also be included if desired.

The extremes of R_E are $0.9 \times 16\ \text{k}\Omega = 14.4\ \text{k}\Omega$, and $1.1 \times 16\ \text{k}\Omega = 17.6\ \text{k}\Omega$. The extreme values of V_{EQ} are somewhat more complicated:

$$V_{EQ} = V_{CC}\frac{R_1}{R_1 + R_2} = \frac{V_{CC}}{1 + \dfrac{R_2}{R_1}} \tag{5.64}$$

To make V_{EQ} as large as possible, the numerator of Eq. (5.64) should be large and the denominator small. Therefore, V_{CC} and R_1 must be as large as possible and R_2 as small as possible. Conversely, to make V_{EQ} as small as possible, V_{CC} and R_1 must be small and R_2 must be large. Using this approach, the maximum and minimum values of V_{EQ} are

$$V_{EQ}^{\max} = \frac{12\ \text{V}(1.05)}{1 + \dfrac{36\ \text{k}\Omega(0.9)}{18\ \text{k}\Omega(1.1)}} = 4.78\ \text{V} \qquad \text{and} \qquad V_{EQ}^{\min} = \frac{12\ \text{V}(0.95)}{1 + \dfrac{36\ \text{k}\Omega(1.1)}{18\ \text{k}\Omega(0.9)}} = 3.31\ \text{V}$$

Substituting these values in Eq. (5.60) gives the following extremes for I_C:

$$I_C^{\max} = \frac{4.78\ \text{V} - 0.7\ \text{V}}{14{,}400\ \Omega} = 283\ \mu\text{A} \qquad \text{and} \qquad I_C^{\min} = \frac{3.31\ \text{V} - 0.7\ \text{V}}{17{,}600\ \Omega} = 148\ \mu\text{A}$$

The worst-case range of V_{CE} will be calculated in a similar manner, but we must be careful to watch for possible cancellation of variables:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \cong V_{CC} - I_C R_C - \frac{V_{EQ} - V_{BE}}{R_E} R_E \tag{5.65}$$

$$V_{CE} \cong V_{CC} - I_C R_C - V_{EQ} + V_{BE}$$

The maximum value of V_{CE} in Eq. (5.65) occurs for minimum I_C and minimum R_C and vice versa. Using (5.65), the extremes of V_{CE} are

$$V_{CE}^{\max} \cong 12\ \text{V}(1.05) - (148\ \mu\text{A})(22\ \text{k}\Omega \times 0.9) - 3.31\ \text{V} + 0.7\ \text{V} = 7.06\ \text{V} \quad \checkmark$$

$$V_{CE}^{\min} \cong 12\ \text{V}(0.95) - (283\ \mu\text{A})(22\ \text{k}\Omega \times 1.1) - 4.78\ \text{V} + 0.7\ \text{V} = 0.471\ \text{Saturated!}$$

Check of Results: The transistor remains in the forward-active region for the upper extreme, but the transistor saturates (weakly) at the lower extreme. Because the forward-active region

assumption is violated in the latter case, the calculated values of V_{CE} and I_C would not actually be correct for this case.

Discussion: Note that the worst-case values of I_C differ by a factor of almost 2:1! The maximum I_C is 38 percent greater than the nominal value of 210 μA, and the minimum value is 37 percent below the nominal value. The failure of the bias circuit to maintain the transistor in the desired region of operation for the worst-case values is evident.

5.12.2 MONTE CARLO ANALYSIS

In a real circuit, the parameters will have some statistical distribution, and it is unlikely that the various components will all reach their extremes at the same time. Thus, the worst-case analysis technique will overestimate (often badly) the extremes of circuit behavior. A better approach is to attack the problem statistically using the method of Monte Carlo analysis.

As discussed in Chapter 1, **Monte Carlo analysis** uses randomly selected versions of a given circuit to predict its behavior from a statistical basis. For Monte Carlo analysis, values for each parameter in the circuit are selected at random from the possible distributions of parameters, and the circuit is then analyzed using the randomly selected element values. Many random parameter sets are generated, and the statistical behavior of the circuit is built up from analysis of the many test cases.

In Ex. 5.12, an Excel spreadsheet will be used to perform a Monte Carlo analysis of the four-resistor bias circuit. As discussed in Chapter 1, Excel contains the function RAND( ), which generates random numbers uniformly distributed between 0 and 1, but for Monte Carlo analysis, the mean must be centered on R_{nom} and the width of the distribution set to $(2\varepsilon) \times R_{\text{nom}}$:

$$R = R_{\text{nom}}[1 + 2\varepsilon(\text{RAND}( ) - 0.5)] \tag{5.66}$$

EXAMPLE 5.12 MONTE CARLO ANALYSIS OF THE FOUR-RESISTOR BIAS NETWORK

Now, let us compare the worst-case results from Ex. 5.11 to a statistical sample of 500 randomly generated realizations of the transistor embedded in the four-resistor bias network.

PROBLEM Perform a Monte Carlo analysis to determine statistical distributions for the collector current and collector-emitter voltage for the four-resistor circuit in Figs. 5.32 and 5.36 with a 5 percent tolerance on V_{CC}, 10 percent tolerances for each resistor and a 50 percent tolerance on the current gain $\beta_{FO} = 75$.

SOLUTION **Known Information and Given Data:** Circuit in Fig. 5.32(a) as simplified in Fig. 5.36; 5 percent tolerance on the 12-V power supply V_{CC}; 10 percent tolerance on each resistor; current $\beta_{FO} = 75$ with a 50 percent tolerance

Unknowns: Statistical distributions of I_C and V_{CE}

Approach: To perform a Monte Carlo analysis of the circuit in Fig. 5.32, random values are assigned to V_{CC}, R_1, R_2, R_C, R_E, and β_F and then used to determine I_C and V_{CE}. A spreadsheet is used to make the repetitive calculations. Since the computer is performing the calculations, the most exact formulas will be used in the analyses.

Assumptions: V_{BE} is fixed at 0.7 V. Random values are statistically independent of each other.

Computer-Aided Analysis: Using the tolerances from the worst-case analysis, the power supply, resistors, and current gain are represented as

$$
\begin{aligned}
&1.\quad V_{CC} = 12(1 + 0.1(\text{RAND}( ) - 0.5))\\
&2.\quad R_1 = 18{,}000(1 + 0.2(\text{RAND}( ) - 0.5))\\
&3.\quad R_2 = 36{,}000(1 + 0.2(\text{RAND}( ) - 0.5))\\
&4.\quad R_E = 16{,}000(1 + 0.2(\text{RAND}( ) - 0.5))\\
&5.\quad R_C = 22{,}000(1 + 0.2(\text{RAND}( ) - 0.5))\\
&6.\quad \beta_F = 75(1 + (\text{RAND}() - 0.5))
\end{aligned}
\tag{5.67}
$$

Remember, each variable evaluation must invoke a separate call of the function RAND( ) so that the random values will be independent of each other.

In the spreadsheet results presented in Fig. 5.37, the random elements in Eq. (5.67) are used to evaluate the equations that characterize the bias circuit:

$$
\begin{aligned}
&7.\quad V_{EQ} = V_{CC}\frac{R_1}{R_1 + R_2} \qquad &&10.\quad I_C = \beta_F I_B\\
&8.\quad R_{EQ} = \frac{R_1 R_2}{R_1 + R_2} \qquad &&11.\quad I_E = \frac{I_C}{\alpha_F}\\
&9.\quad I_B = \frac{V_{EQ} - V_{BE}}{R_{EQ} + (\beta_F + 1)R_E} \qquad &&12.\quad V_{CE} = V_{CC} - I_C R_C - I_E R_E
\end{aligned}
\tag{5.68}
$$

Because the computer is doing the work, the complete expressions rather than the approximate relations for the various calculations are used in Eq. (5.68).[10] Once Eqs. (5.67) and (5.68) have been entered into one row of the spreadsheet, that row can be copied into as many additional rows as the number of statistical cases that are desired. The analysis is automatically repeated for the random selections to build up the statistical distributions, with each row representing one analysis of the circuit. At the end of the columns, the mean and standard deviation can be calculated using built-in spreadsheet functions, and the overall spreadsheet data can be used to build histograms for the circuit performance.

An example of a portion of the spreadsheet output for 25 cases of the circuit in Fig. 5.36 is shown in Fig. 5.37, whereas the full results of the analysis of 500 cases of the four-resistor bias circuit are given in the histograms for I_C and V_{CE} in Fig. 5.38. The mean values for I_C and V_{CE} are 207 μA and 4.06 V, respectively, which are close to the values originally estimated from the nominal circuit elements. The standard deviations are 19.6 μA and 0.64 V, respectively.

Check of Results and Discussion: The worst-case calculations from Sec. 5.12.1 are indicated by the arrows in the figures. It can be seen that the worst-case values of V_{CE} lie well beyond the edges of the statistical distribution, and that saturation does not actually occur for the worst statistical case evaluated. If the Q-point distribution results in the histograms in Fig. 5.38 were not sufficient to meet the design criteria, the parameter tolerances could be changed and the Monte Carlo simulation redone. For example, if too large a fraction of the circuits failed to be within some specified limits, the tolerances could be tightened by specifying more expensive, higher accuracy resistors.

[10]Note that V_{BE} could also be treated as a random variable.

Monte Carlo Spreadsheet

Case #	V_{CC} (1)	R_1 (2)	R_2 (3)	R_E (4)	R_C (5)	β_F (6)	V_{EQ} (7)	R_{EQ} (8)	I_B (9)	I_C (10)	V_{CE} (12)
1	12.277	16827	38577	15780	23257	67.46	3.729	11716	2.87E-06	1.93E-04	4.687
2	12.202	18188	32588	15304	23586	46.60	4.371	11673	5.09E-06	2.37E-04	2.891
3	11.526	16648	35643	14627	20682	110.73	3.669	11348	1.87E-06	2.07E-04	4.206
4	11.658	17354	33589	14639	22243	44.24	3.971	11442	5.00E-06	2.21E-04	3.420
5	11.932	19035	32886	16295	20863	62.34	4.374	12056	3.61E-06	2.25E-04	3.500
6	11.857	18706	32615	15563	21064	60.63	4.322	11888	3.83E-06	2.32E-04	3.286
7	11.669	18984	39463	17566	21034	42.86	3.790	12818	4.07E-06	1.75E-04	4.859
8	12.222	19291	37736	15285	22938	63.76	4.135	12765	3.53E-06	2.25E-04	3.577
9	11.601	17589	34032	17334	23098	103.07	3.953	11596	1.85E-06	1.90E-04	3.873
10	11.533	17514	33895	17333	19869	71.28	3.929	11547	2.63E-06	1.88E-04	4.505
11	11.436	19333	34160	15107	22593	68.20	4.133	12346	3.34E-06	2.28E-04	2.797
12	11.962	18810	33999	15545	22035	53.69	4.261	12110	4.25E-06	2.28E-04	3.330
13	11.801	19610	37917	14559	21544	109.65	4.023	12925	2.11E-06	2.31E-04	3.426
14	12.401	17947	34286	15952	21086	107.84	4.261	11780	2.09E-06	2.26E-04	4.002
15	11.894	16209	35321	17321	23940	45.00	3.741	11111	3.89E-06	1.75E-04	4.607
16	12.329	16209	37873	16662	23658	112.01	3.695	11351	1.63E-06	1.83E-04	4.923
17	11.685	19070	35267	15966	21864	64.85	4.101	12377	3.29E-06	2.13E-04	3.559
18	11.456	18096	37476	15529	20141	91.14	3.730	12203	2.17E-06	1.98E-04	4.370
19	12.527	18752	38261	15186	21556	69.26	4.120	12584	3.26E-06	2.26E-04	4.180
20	12.489	17705	36467	17325	20587	83.95	4.082	11919	2.35E-06	1.97E-04	4.979
21	11.436	18773	34697	16949	21848	65.26	4.015	12182	3.01E-06	1.96E-04	3.768
22	11.549	16830	38578	16736	19942	109.22	3.508	11718	1.57E-06	1.71E-04	5.247
23	11.733	16959	39116	15944	21413	62.82	3.548	11830	2.86E-06	1.80E-04	4.965
24	11.738	18486	35520	17526	20455	70.65	4.018	12158	2.70E-06	1.90E-04	4.457
25	11.679	18908	38236	15160	21191	103.12	3.864	12652	2.05E-06	2.12E-04	3.958
Mean	11.848	18014	35102	15973	21863	67.30	4.024	11885	3.44E-06	2.09E-04	3.880
Std. Dev.	0.296	958	2596	1108	1309	23.14	0.264	520	1.14E-06	2.18E-05	0.657

(X) = Equation number in text

Figure 5.37 Example of a Monte Carlo analysis using a spreadsheet.

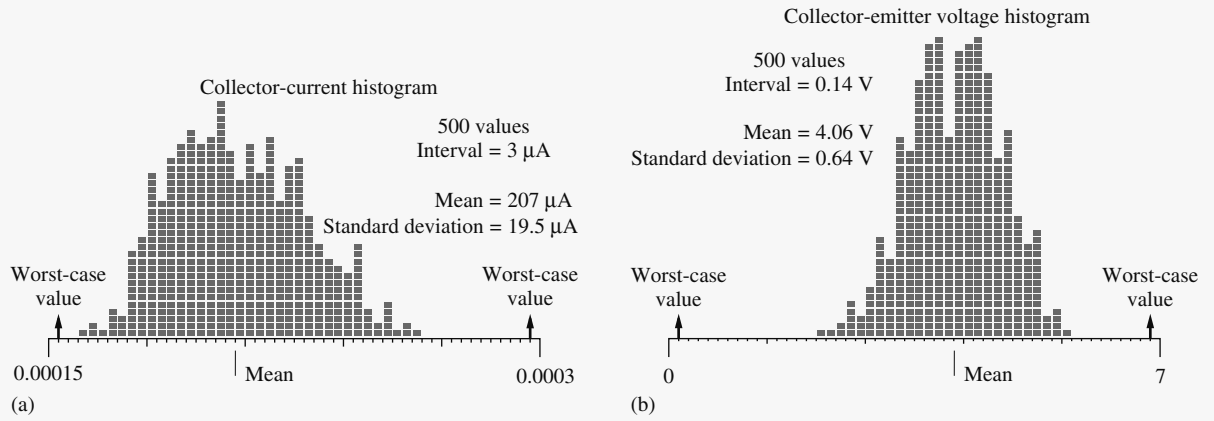


Figure 5.38 (a) Collector-current histogram; (b) collector-emitter voltage histogram.

Some implementations of the SPICE circuit analysis program actually contain a Monte Carlo option in which a full circuit simulation is automatically performed for any number of randomly selected test cases. These programs are a powerful tool for performing much more complex statistical analysis than is possible by hand. Using these programs, statistical estimates of delay, frequency response, and so on of circuits with large numbers of transistors can be performed.

SUMMARY

- The bipolar junction transistor (BJT) was invented in the late 1940s at the Bell Telephone Laboratories by Bardeen, Brattain, and Shockley and became the first commercially successful three-terminal solid-state device.
- Although the FET has become the dominant device technology in modern integrated circuits, bipolar transistors are still widely used in both discrete and integrated circuit design. In particular, the BJT is still the preferred device in many applications that require high speed and/or high precision such as op-amps, A/D and D/A converters, and wireless communication products.
- The basic physical structure of the BJT consists of a three-layer sandwich of alternating p- and n-type semiconductor materials and can be fabricated in either *npn* or *pnp* form.
- The emitter of the transistor injects carriers into the base. Most of these carriers traverse the base region and are collected by the collector. The carriers that do not completely traverse the base region give rise to a small current in the base terminal.
- A mathematical model called the transport model (a simplified Gummel-Poon model) characterizes the i-v characteristics of the bipolar transistor for general terminal voltage and current conditions. The transport model requires three unique parameters to characterize a particular BJT: saturation current I_S and forward and reverse common-emitter current gains β_F and β_R.
- β_F is a relatively large number, ranging from 20 to 500, and characterizes the significant current amplification capability of the BJT. Practical fabrication limitations cause the bipolar transistor structure to be inherently asymmetric, and the value of β_R is much smaller than β_F, typically between 0 and 10.

- SPICE circuit analysis programs contain a comprehensive built-in model for the transistor that is an extension of the transport model.
- Four regions of operation — cutoff, forward-active, reverse-active, and saturation — were identified for the BJT based on the bias voltages applied to the base-emitter and base-collector junctions. The transport model can be simplified for each individual region of operation.
- The cutoff and saturation regions are most often used in switching applications and logic circuits. In cutoff, the transistor approximates an open switch, whereas in saturation, the transistor represents a closed switch. However, in contrast to the "on" MOSFET, the saturated bipolar transistor has a small voltage, the collector-emitter saturation voltage V_{CESAT}, between its collector and emitter terminals, even when operating with zero collector current.
- In the forward-active region, the bipolar transistor can provide high voltage and current gain for amplification of analog signals. The reverse-active region finds limited use in some analog- and digital-switching applications.
- The i-v characteristics of the bipolar transistor are often presented graphically in the form of the output characteristics, i_C versus v_{CE} or v_{CB}, and the transfer characteristics, i_C versus v_{BE} or v_{EB}.
- In the forward-active region, the collector current increases slightly as the collector-emitter voltage increases. The origin of this effect is base-width modulation, known as the Early effect, and it can be included in the model for the forward-active region through addition of the parameter called the Early voltage V_A.
- The collector current of the bipolar transistor is determined by minority-carrier diffusion across the base of the transistor, and expressions were developed that relate the saturation current and base transit time of the transistor to physical device parameters. The base width plays a crucial role in determining the base transit time and the high-frequency operating limits of the transistor.
- Minority-carrier charge is stored in the base of the transistor during its operation, and changes in this stored charge with applied voltage result in diffusion capacitances being associated with forward-biased junctions. The value of the diffusion capacitance is proportional to the collector current I_C.
- Capacitances of the bipolar transistor cause the current gain to be frequency-dependent. At the beta cutoff frequency f_β, the current gain has fallen to 71 percent of its low frequency value, whereas the value of the current gain is only 1 at the unity-gain frequency f_T.
- The transconductance g_m of the bipolar transistor in the forward-active region relates differential changes in collector current and base-emitter voltage and was shown to be directly proportional to the dc collector current I_C.
- Design of the four-resistor network was investigated in detail. The four-resistor bias circuit provides highly stable control of the Q-point and is the most important bias circuit for discrete design.
- Techniques for analyzing the influence of element tolerances on circuit performance include the worst-case analysis and statistical Monte Carlo analysis methods. In worst-case analysis, element values are simultaneously pushed to their extremes, and the resulting predictions of circuit behavior are often overly pessimistic. The Monte Carlo method analyzes a large number of randomly selected versions of a circuit to build up a realistic estimate of the statistical distribution of circuit performance. Random number generators in high-level computer languages, spreadsheets, or MATLAB can be used to randomly select element values for use in the Monte Carlo analysis. Some circuit analysis packages such as PSPICE provide a Monte Carlo analysis option as part of the program.

KEY TERMS

Base
Base current
Base width
Base-collector capacitance
Base-emitter capacitance
Base-width modulation
β-cutoff frequency f_β
Bipolar junction transistor (BJT)
Collector
Collector current
Common-base output characteristic
Common-emitter output characteristic
Common-emitter transfer characteristic
Cutoff region
Diffusion capacitance
Early effect
Early voltage V_A
Ebers-Moll model
Emitter
Emitter current
Equilibrium electron density
Forced beta
Forward-active region
Forward common-emitter current gain β_F
Forward common-base current gain α_F
Forward transit time τ_F
Forward transport current
Gummel-Poon model
Inverse-active region
Inverse common-emitter current gain
Inverse common-base current gain
Monte Carlo analysis
Normal-active region
Normal common-emitter current gain
Normal common-base current gain
npn transistor
Output characteristic
pnp transistor
Quiescent operating point
Q-point
Reverse-active region
Reverse common-base current gain α_R
Reverse common-emitter current gain β_R
Saturation region
Saturation voltage
SPICE model parameters BF, IS, VAF
Transconductance
Transfer characteristic
Transistor saturation current
Transport model
Unity-gain frequency f_T
Worst-case analysis

REFERENCES

1. William F. Brinkman, "The transistor: 50 glorious years and where we are going," *IEEE International Solid-State Circuits Conference Digest,* vol. 40, pp. 22–26, February 1997.
2. William F. Brinkman, Douglas E. Haggan, William W. Troutman, "A history of the invention of the transistor and where it will lead us," *IEEE Journal of Solid-State Circuits,* vol. 32, pp. 1858–1865, December 1997.
3. H. K. Gummel and H. C. Poon, "A compact bipolar transistor model," *ISSCC Digest of Technical Papers,* pp. 78, 79, 146, February 1970.
4. H. K. Gummel, "A charge control relation for bipolar transistors," *Bell System Technical Journal,* January 1970.
5. J. J. Ebers and J. L. Moll, "Large signal behavior of junction transistors," *Proc. IRE.,* pp. 1761–1772, December 1954.
6. R. C. Jaeger and A. J. Brodersen, "Self consistent bipolar transistor models for computer simulation," *Solid-State Electronics*, vol. 21, no. 10, pp. 1269–1272, October 1978.
7. J. M. Early, "Effects of space-charge layer widening in junction transistors," *Proc. IRE.,* pp. 1401–1406, November 1952.
8. B. M. Wilamowski and R. C. Jaeger, *Computerized Circuit Analysis Using SPICE Programs,* McGraw-Hill, New York: 1997.
9. J. D. Cressler, "Reengineering silicon: S_iG_e heterojunction bipolar technology," *IEEE Spectrum,* pp. 49–55, March 1995.

PROBLEMS

If not otherwise specified, use $I_S = 10^{-16}$ A, $V_A = 50$ V, $\beta_F = 100$, $\beta_R = 1$, and $V_{BE} = 0.70$ V.

5.1 Physical Structure of the Bipolar Transistor

5.1. Figure P5.1 is a cross section of an *npn* bipolar transistor similar to that in Fig. 5.1. Indicate the letter (*A* to *G*) that identifies the base contact, collector contact, emitter contact, *n*-type emitter region, *n*-type collector region, and the active or intrinsic transistor region.

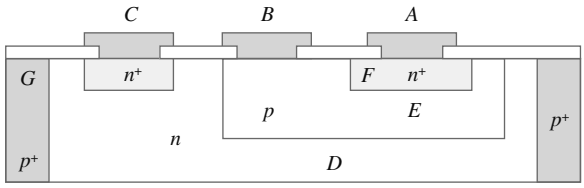


Figure P5.1

5.2 The Transport Model for the *npn* Transistor

5.2. (a) Label the collector, base, and emitter terminals of the transistor in the circuit in Fig. P5.2. (b) Label the base-emitter and base-collector voltages, V_{BE} and V_{BC}, respectively. (c) If $V = 0.650$ V, $I_C = 275\,\mu$A, and $I_B = 3\,\mu$A, find the values of I_S, β_F, and β_R for the transistor if $\alpha_R = 0.55$.

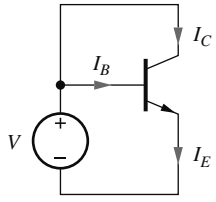


Figure P5.2

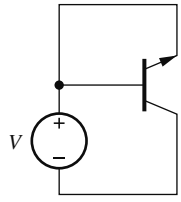


Figure P5.3

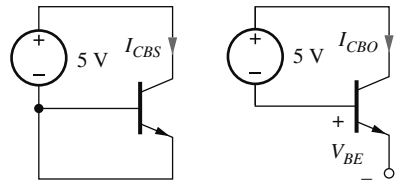
5.3. (a) Label the collector, base, and emitter terminals of the transistor in the circuit in Fig. P5.3. (b) Label the base-emitter and base-collector voltages, V_{BE} and V_{BC}, and the positive directions of the collector, base, and emitter currents. (c) If $V = 0.615$ V, $I_E = -275\,\mu$A, and $I_B = 125\,\mu$A, find the values of I_S, β_F, and β_R for the transistor if $\alpha_F = 0.975$.

5.4. Fill in the missing entries in Table P5.4

TABLE P5.4

α	β
	0.200
0.400	
0.750	
	10.0
0.980	
	200
	1000
0.9998	

5.5. (a) Find the current I_{CBS} in Fig. P5.5(a). (Use the parameters specified at the beginning of the problem set.) (b) Find the current I_{CBO} and the voltage V_{BE} in Fig. P5.5(b).



(a) (b)

Figure P5.5

5.6. For the transistor in Fig. P5.6, $I_S = 5 \times 10^{-16}$ A, $\beta_F = 100$, and $\beta_R = 0.25$. (a) Label the collector, base, and emitter terminals of the transistor. (b) What is the transistor type? (c) Label the base-emitter and base-collector voltages, V_{BE} and V_{BC}, respectively, and label the normal directions for I_E, I_C, and I_B. (d) What is the relationship between V_{BE} and V_{BC}? (e) Write the simplified form of the transport model equations that apply to this particular circuit configuration. Write an expression for I_E/I_B. Write an expression for I_E/I_C. (f) Find the values of I_E, I_C, I_B, V_{BC}, and V_{BE}.

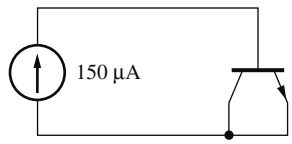


Figure P5.6

5.7. For the transistor in Fig. P5.7, $I_S = 6 \times 10^{-16}$ A, $\beta_F = 100$, and $\beta_R = 0.25$. (a) Label the collector, base, and emitter terminals of the transistor. (b) What is the transistor type? (c) Label the base-emitter and base-collector voltages, V_{BE} and V_{BC}, and the normal directions for I_E, I_C, and I_B. (d) Find the values of I_E, I_C, I_B, V_{BC}, and V_{BE} if $I = 175$ μA.

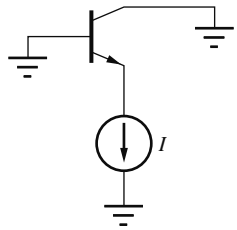


Figure P5.7

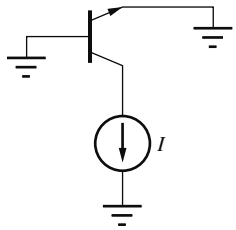


Figure P5.8

5.8. For the transistor in Fig. P5.8, $I_S = 6 \times 10^{-16}$ A, $\beta_F = 100$, and $\beta_R = 0.25$. (a) Label the collector, base, and emitter terminals of the transistor. (b) What is the transistor type? (c) Label the base-emitter and base-collector voltages, V_{BE} and V_{BC}, and label the normal directions for I_E, I_C, and I_B. (d) Find the values of I_E, I_C, I_B, V_{BC}, and V_{BE} if $I = 175$ μA.

5.9. The *npn* transistor is connected in a "diode" configuration in Fig. P5.9(a). Use the transport model equations to show that the *i-v* characteristics of this connection are similar to those of a diode as defined by Eq. (3.11). What is the reverse saturation current of this "diode" if $I_S = 4 \times 10^{-15}$ A, $\beta_F = 100$, and $\beta_R = 0.25$?

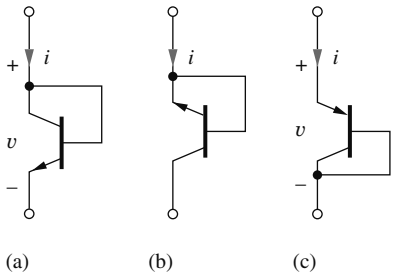


Figure P5.9

5.10. The *npn* transistor is connected in an alternate "diode" configuration in Fig. P5.9(b). Use the transport model equations to show that the *i-v* characteristics of this connection are similar to those of a diode as defined by Eq. (3.11). What is the reverse saturation current of this "diode" if $I_S = 5 \times 10^{-16}$ A, $\beta_F = 60$, and $\beta_R = 3$?

5.11. Calculate i_T for an *npn* transistor with $I_S = 10^{-15}$ A for (a) $V_{BE} = 0.70$ V and $V_{BC} = -3$ V and (b) $V_{BC} = 0.70$ V and $V_{BE} = -3$ V.

5.12. Calculate i_T for an *npn* transistor with $I_S = 10^{-16}$ A for (a) $V_{BE} = 0.75$ V and $V_{BC} = -3$ V and (b) $V_{BC} = 0.75$ V and $V_{BE} = -3$ V.

5.3 The *pnp* Transistor

5.13. Figure P5.13 is a cross section of a *pnp* bipolar transistor similar to the *npn* transistor in Fig. 5.1. Indicate the letter (*A* to *G*) that represents the base contact, collector contact, emitter contact, *p*-type emitter region, *p*-type collector region, and the active or intrinsic transistor region.

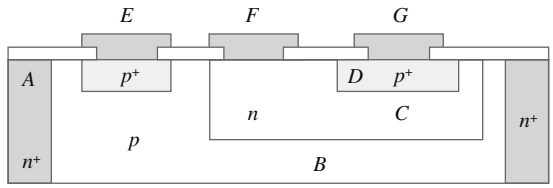


Figure P5.13

5.14. For the transistor in Fig. P5.14(a), $I_S = 6 \times 10^{-16}$ A, $\alpha_F = 0.985$, and $\alpha_R = 0.25$. (a) What type of transistor is in this circuit? (b) Label the collector, base, and emitter terminals of the transistor. (c) Label the emitter-base and collector-base voltages, and label the normal direction for I_E, I_C, and I_B. (d) Write the simplified form of the transport model equations that apply to this particular circuit configuration. Write an expression for I_E/I_C. Write an expression for I_E/I_B. (e) Find the values of I_E, I_C, I_B, β_F, β_R, V_{EB}, and V_{CB}.

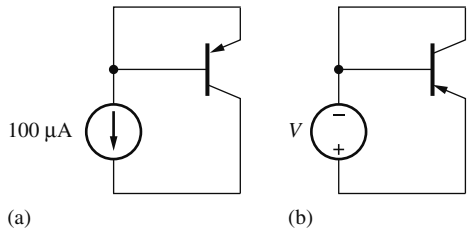


Figure P5.14

5.15. (a) Label the collector, base, and emitter terminals of the transistor in the circuit in Fig. P5.14(b). (b) Label the emitter-base and collector-base voltages, V_{EB} and V_{CB}, and the normal directions for I_E, I_C, and I_B. (c) If $V = 0.640$ V, $I_C = 300$ μA,

and $I_B = 4\ \mu A$, find the values of I_S, β_F, and β_R for the transistor if $\alpha_R = 0.2$.

5.16. Repeat Prob. 5.9 for the "diode-connected" *pnp* transistor in Fig. P5.9(c).

5.17. For the transistor in Fig. P5.17, $I_S = 4 \times 10^{-16}$ A, $\beta_F = 75$, and $\beta_R = 4$. (a) Label the collector, base, and emitter terminals of the transistor. (b) What is the transistor type? (c) Label the emitter-base and collector-base voltages, and label the normal direction for I_E, I_C, and I_B. (d) Write the simplified form of the transport model equations that apply to this particular circuit configuration. Write an expression for I_E/I_B. Write an expression for I_E/I_C. (e) Find the values of I_E, I_C, I_B, V_{CB}, and V_{EB}.

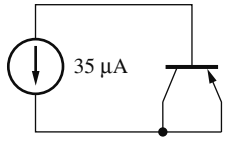


Figure P5.17

5.18. For the transistor in Fig. P5.18(a), $I_S = 2.5 \times 10^{-16}$ A, $\beta_F = 100$, and $\beta_R = 5$. (a) Label the collector, base, and emitter terminals of the transistor. (b) What is the transistor type? (c) Label the emitter-base and collector-base voltages, V_{EB} and V_{CB}, and the normal directions for I_E, I_C, and I_B. (d) Find the values of I_E, I_C, I_B, V_{CB}, and V_{EB} if $I = 300\ \mu A$.

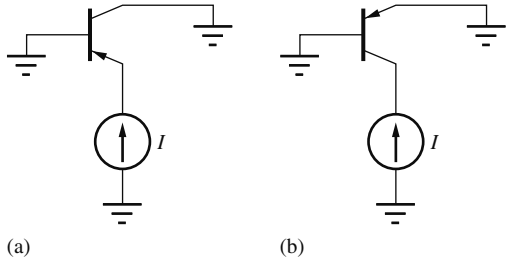


Figure P5.18

5.19. For the transistor in Fig. P5.18(b), $I_S = 2.5 \times 10^{-16}$ A, $\beta_F = 75$, and $\beta_R = 1$. (a) Label the collector, base, and emitter terminals of the transistor. (b) What is the transistor type? (c) Label the emitter-base and collector-base voltages, V_{EB} and V_{CB}, and label the normal directions for I_E, I_C, and I_B. (d) Find the values of I_E, I_C, I_B, V_{CB}, and V_{EB} if $I = 300\ \mu A$.

5.20. Calculate i_T for a *pnp* transistor with $I_S = 6 \times 10^{-16}$ A for (a) $V_{EB} = 0.70$ V and $V_{CB} = -3$ V and (b) $V_{CB} = 0.70$ V and $V_{EB} = -3$ V.

5.4 Equivalent Circuit Representations for the Transport Models

5.21. Calculate the values of i_T and the two diode currents for the equivalent circuit in Fig. 5.8(a) for an *npn* transistor with $I_S = 2.5 \times 10^{-16}$ A, $\beta_F = 80$, and $\beta_R = 2$ for (a) $V_{BE} = 0.73$ V and $V_{BC} = -3$ V and (b) $V_{BC} = 0.73$ V and $V_{BE} = -3$ V.

5.22. Calculate the values of i_T and the two diode currents for the equivalent circuit in Fig. 5.8(b) for a *pnp* transistor with $I_S = 4 \times 10^{-15}$A, $\beta_F = 60$, and $\beta_R = 3$ for (a) $V_{EB} = 0.68$ V and $V_{CB} = -3$ V and (b) $V_{CB} = 0.68$ V and $V_{EB} = -3$ V.

5.23. The Ebers-Moll model was one of the first mathematical models used to describe the characteristics of the bipolar transistor. Show that the *npn* transport model equations can be transformed into the Ebers-Moll equations below. [*Hint:* Add and subtract 1 from the collector and emitter current expressions in Eqs. (5.13).]

$$i_E = I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] - \alpha_R I_{CS}\left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1\right]$$

$$i_C = \alpha_F I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] - I_{CS}\left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1\right]$$

$$i_B = (1-\alpha_F) I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] + (1-\alpha_R) I_{CS}\left[\exp\left(\frac{v_{BC}}{V_T}\right) - 1\right]$$

$$\alpha_F I_{ES} = \alpha_R I_{CS}$$

5.24. What are the values of α_F, α_R, I_{ES}, and I_{CS} for an *npn* transistor with $I_S = 4 \times 10^{-15}$ A, $\beta_F = 100$, and $\beta_R = 0.5$? Show that $\alpha_F I_{ES} = \alpha_R I_{CS}$.

5.25. The Ebers-Moll model was one of the first mathematical models used to describe the characteristics of the bipolar transistor. Show that the *pnp* transport model equations can be transformed into the Ebers-Moll equations that follow. [*Hint*: Add and subtract 1 from the collector and emitter current expressions in Eqs. (5.17).]

$$i_E = I_{ES}\left[\exp\left(\frac{v_{EB}}{V_T}\right) - 1\right] - \alpha_R I_{CS}\left[\exp\left(\frac{v_{CB}}{V_T}\right) - 1\right]$$

$$i_C = \alpha_F I_{ES}\left[\exp\left(\frac{v_{EB}}{V_T}\right) - 1\right] - I_{CS}\left[\exp\left(\frac{v_{CB}}{V_T}\right) - 1\right] \qquad \alpha_F I_{ES} = \alpha_R I_{CS}$$

$$i_B = (1-\alpha_F) I_{ES}\left[\exp\left(\frac{v_{EB}}{V_T}\right) - 1\right] + (1-\alpha_R) I_{CS}\left[\exp\left(\frac{v_{CB}}{V_T}\right) - 1\right]$$

5.5 The i-v Characteristics of the Bipolar Transistor

*5.26. The common-emitter output characteristics for an *npn* transistor are given in Fig. P5.26. What are the values of β_F at (a) $I_C = 5$ mA and $V_{CE} = 5$ V? (b) $I_C = 7$ mA and $V_{CE} = 7.5$ V? (c) $I_C = 10$ mA and $V_{CE} = 14$ V?

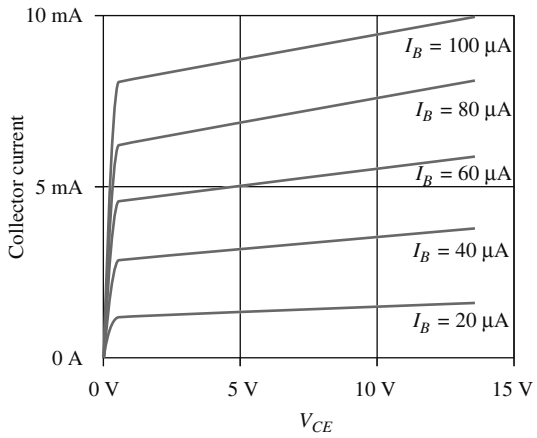


Figure P5.26

5.27. Plot the common-emitter output characteristics for an *npn* transistor having $I_S = 1$ fA, $\beta_{FO} = 75$, and $V_A = 50$ V for six equally spaced base current steps ranging from 0 to 200 μA and V_{CE} ranging from 0 to 10 V.

5.28. Use SPICE to plot the common-emitter output characteristics for the *npn* transistor in Prob. 5.27.

5.29. Plot the common-emitter output characteristics for a *pnp* transistor having $I_S = 1$ fA, $\beta_{FO} = 75$, and $V_A = 50$ V for six equally spaced base current steps ranging from 0 to 250 μA and V_{EC} ranging from 0 to 10 V.

5.30. Use SPICE to plot the common-emitter output characteristics for the *pnp* transistor in Prob. 5.29.

5.31. What is the reciprocal of the slope (in mV/decade) of the logarithmic transfer characteristic for an *npn* transistor in the common-emitter configuration at a temperature of (a) 200 K, (b) 250 K, (c) 300 K, and (d) 350 K?

Junction Breakdown Voltages

*5.32. In the circuits in Fig. P5.9, the Zener breakdown voltages of the collector-base and emitter-base junctions of the transistors are 40 V and 5 V, respectively. What is the Zener breakdown voltage for each "diode" connected transistor configuration?

5.33. In the circuits in Fig. P5.33, the Zener breakdown voltages of the collector-base and emitter-base junctions of the *npn* transistors are 40 V and 6.3 V, respectively. What is the current in the resistor in each circuit? (*Hint:* The equivalent circuits for the transport model equations may help in visualizing the circuit.)

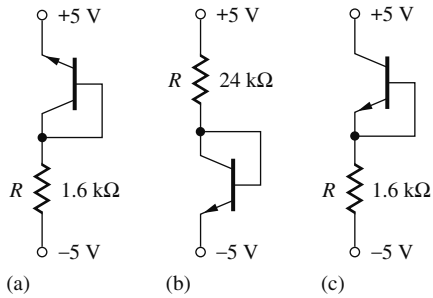


Figure P5.33

5.34. An *npn* transistor is biased as indicated in Fig. 5.9(a). What is the largest value of V_{CE} that can be applied without junction breakdown if the breakdown voltages of the collector-base and emitter-base junctions of the *npn* transistors are 60 V and 5 V, respectively?

*5.35. (a) For the circuit in Fig. P5.35, what is the maximum value of I according to the transport model equations if $I_S = 1 \times 10^{-16}$ A, $\beta_F = 50$, and $\beta_R = 0.5$? (b) Suppose that $I = 1$ mA. What happens to the transistor? (*Hint:* The equivalent circuits for the transport model equations may help in visualizing the circuit.)

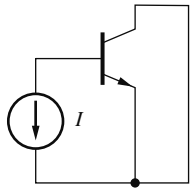


Figure P5.35

5.6 The Operating Regions of the Bipolar Transistor

5.36. Indicate the region of operation in the following table for an *npn* transistor biased with the indicated voltages.

BASE-EMITTER VOLTAGE	BASE-COLLECTOR VOLTAGE	
	0.7 V	−5.0 V
−5.0 V		
0.7 V		

5.37. (a) What are the regions of operation for the transistors in Fig. P5.9? (b) In Fig. P5.44(a)? (c) In Fig. P5.47? (d) In Fig. P5.60?

5.38. (a) What is the region of operation for the transistor in Fig. P5.5(a)? (b) In Fig. P5.5(b)?

5.39. (a) What is the region of operation for the transistor in Fig. P5.6? (b) In Fig. P5.7? (c) In Fig. P5.8?

5.40. Indicate the region of operation in the following table for a *pnp* transistor biased with the indicated voltages.

EMITTER-BASE VOLTAGE	COLLECTOR-BASE VOLTAGE	
	0.7 V	−0.65 V
0.7 V		
−0.65 V		

5.41. (a) What is the region of operation for the transistor in Fig. P5.2? (b) In Fig. P5.3?

5.42. (a) What is the region of operation for the transistor in Fig. P5.14(a)? (b) In Fig. P5.14(b)?

5.43. (a) What is the region of operation for the transistor in Fig. P5.17? (b) In Fig. P5.18(a)? (c) In Fig. P5.18(b).

5.7 Transport Model Simplifications

Cutoff Region

5.44. (a) What are the three terminal currents I_E, I_B, and I_C in the transistor in Fig. P5.44(a) if $I_S = 2 \times 10^{-16}$ A, $\beta_F = 75$, and $\beta_R = 4$? (b) Repeat for Fig. P5.44(b).

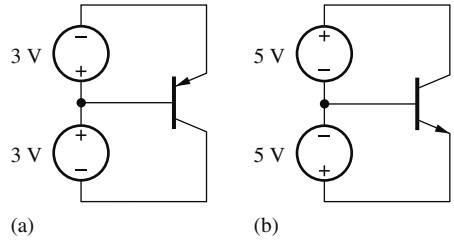


Figure P5.44

**5.45. An *npn* transistor with $I_S = 5 \times 10^{-16}$ A, $\alpha_F = 0.95$, and $\alpha_R = 0.5$ is operating with $V_{BE} = 0.3$ V and $V_{BC} = -5$ V. This transistor is not truly operating in the region defined to be cutoff, but we still say the transistor is off. Why? Use the transport model equations to justify your answer. In what region is the transistor actually operating according to our definitions?

Forward-Active Region

5.46. What are the values of β_F and I_S for the transistor in Fig. P5.46?

5.47. What are the values of β_F and I_S for the transistor in Fig. P5.47?

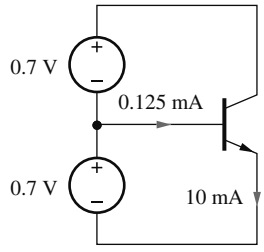


Figure P5.46

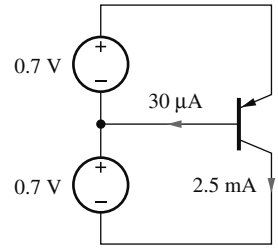


Figure P5.47

5.48. What are the emitter, base, and collector currents in the circuit in Fig. 5.16 if $V_{EE} = 3.3$ V, $R = 47$ kΩ, and $\beta_F = 80$?

**5.49. A transistor has $f_T = 500$ MHz and $\beta_F = 75$. (a) What is the β-cutoff frequency f_β of this transistor? (b) Use Eq. (5.41) to find an expression for the frequency dependence of α_F — that is, $\alpha_F(f)$. [*Hint:* Write an expression for $\beta(s)$.] What is the α-cutoff frequency for this transistor?

*5.50. (a) Start with the transport model equations for the *pnp* transistor, Eq. (5.17), and construct the simplified version of the *pnp* equations that apply to the forward-active region [similar to Eq. (5.23)]. (b) Draw the simplified model for the *pnp* transistor similar to the *npn* version in Fig. 5.19(c).

Reverse-Active Region

5.51. What are the values of β_R and I_S for the transistor in Fig. P5.51?

5.52. What are the values of β_R and I_S for the transistor in Fig. P5.52?

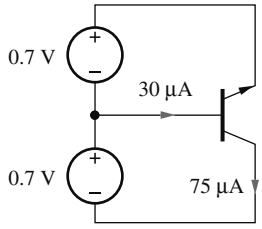


Figure P5.51

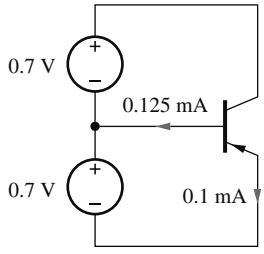


Figure P5.52

5.53. Find the emitter, base, and collector currents in the circuit in Fig. 5.20 if the negative power supply is −3.3 V, $R = 56\ \text{k}\Omega$, and $\beta_R = 0.75$.

Saturation Region

5.54. What is the saturation voltage of an *npn* transistor operating with $I_C = 1$ mA and $I_B = 1$ mA if $\beta_F = 50$ and $\beta_R = 3$? What is the forced β of this transistor? What is the value of V_{BE} if $I_S = 10^{-15}$ A?

5.55. Derive an expression for the saturation voltage V_{ECSAT} of the *pnp* transistor in a manner similar to that used to derive Eq. (5.29).

5.56. (a) What is the collector-emitter voltage for the transistor in Fig. P5.56(a) if $I_S = 7 \times 10^{-16}$ A, $\alpha_F = 0.99$, and $\alpha_R = 0.5$? (b) What is the emitter-collector voltage for the transistor in Fig. P5.56(b) for the same transistor parameters?

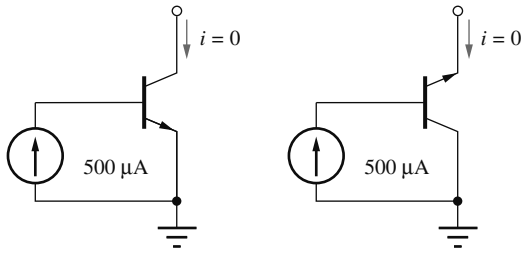


Figure P5.56

5.57. Repeat Prob. 5.56 for $\alpha_F = 0.95$ and $\alpha_R = 0.33$.

5.58. (a) What base current is required to achieve a saturation voltage of $V_{\text{CESAT}} = 0.1$ V in an *npn* power transistor that is operating with a collector current of 20 A if $\beta_F = 20$ and $\beta_R = 0.9$? What is the forced β of this transistor? (b) Repeat for $V_{\text{CESAT}} = 0.04$ V.

**5.59. An *npn* transistor with $I_S = 1 \times 10^{-16}$ A, $\alpha_F = 0.975$, and $\alpha_R = 0.5$ is operating with $V_{BE} = 0.70$ V and $V_{BC} = 0.50$ V. By definition, this transistor is operating in the saturation region. However, in the discussion of Fig. 5.17 it was noted that this transistor actually behaves as if it is still in the forward-active region even though $V_{BC} > 0$. Why? Use the transport model equations to justify your answer.

5.60. The current I in both circuits in Fig. P5.60 is 200 μA. Find the value of V_{BE} for both circuits if $I_S = 4 \times 10^{-16}$ A, $\beta_F = 50$, and $\beta_R = 0.5$. What is V_{CESAT} in Fig. P5.60(b)?

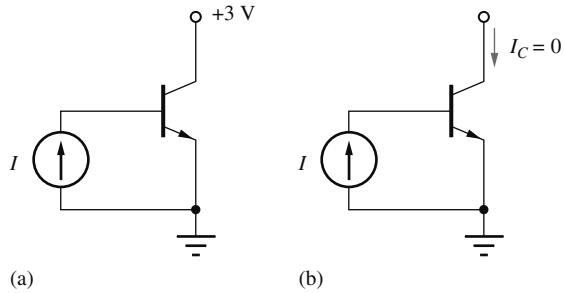


Figure P5.60

Diodes in Bipolar Integrated Circuits

5.61. Derive the result in Eq (5.25) by applying the circuit constraints to the transport equations.

5.62. What is the reverse saturation current of the diode in Fig. 5.18 if the transistor is described by $I_s = 3 \times 10^{-15}$ A, $\alpha_R = 0.20$, and $\alpha_F = 0.98$?

5.63. The two transistors in Fig. P5.63 are identical. What is the collector current of Q_2 if $I = 25$ μA and $\beta_F = 60$?

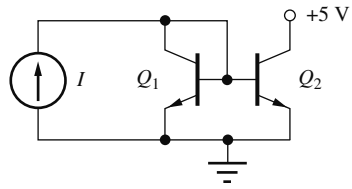


Figure P5.63

5.8 Nonideal Behavior of the Bipolar Transistor

5.64. Calculate the diffusion capacitance of a bipolar transistor with a forward transit time $\tau_F = 50$ ps

for collector currents of (a) 2 μA, (b) 200 μA, (c) 20 mA.

5.65. (a) What is the forward transit time τ_F for an *npn* transistor with a base width $W_B = 0.5$ μm and a base doping of $10^{18}/\text{cm}^3$? (b) Repeat the calculation for a *pnp* transistor.

5.66. What is the diffusion capacitance for an *npn* transistor with $\tau_F = 10$ ps if it is operating at 300 K with a collector currents of 1 μA, 1 mA, and 10 mA?

5.67. A transistor has $f_T = 750$ MHz and $f_\beta = 5$MHz. What is the dc current gain of the transistor? What is the current gain of the transistor at 50 MHz? At 250 MHz?

5.68. A transistor has a dc current gain of 180 and a current gain of 10 at 75 MHz. What are the unity-gain and beta-cutoff frequencies of the transistor?

5.69. An *npn* transistor is needed that will operate at a frequency of at least 5 GHz. What base width is required for the transistor if the base doping is $5 \times 10^{18}/\text{cm}^3$?

5.70. What is the saturation current for a transistor with a base doping of $6 \times 10^{18}/\text{cm}^3$, a base width of 0.25 μm, and a cross-sectional area of 25 μm^2?

The Early Effect and Early Voltage

5.71. An *npn* transistor is operating in the forward-active region with a base current of 3 μA. It is found that $I_C = 225$ μA for $V_{CE} = 5$ V and $I_C = 265$ μA for $V_{CE} = 10$ V. What are the values of β_{FO} and V_A for this transistor?

5.72. An *npn* transistor with $I_S = 5 \times 10^{-16}$ A, $\beta_F = 100$, and $V_A = 65$ V is biased in the forward-active region with $V_{BE} = 0.72$ V and $V_{CE} = 10$ V. (a) What is the collector current I_C? (b) What would be the collector current I_C if $V_A = \infty$? (c) What is the ratio of the two answers in parts (a) and (b)?

5.73. The common-emitter output characteristics for an *npn* transistor are given in Fig. P5.26. What are the values of β_{FO} and V_A for this transistor?

5.74. (a) Recalculate the currents in the transistor in Fig. 5.14 if $I_S = 5 \times 10^{-16}$ A, $\beta_{FO} = 19$, and $V_A = 50$ V. What is V_{BE}? (b) What was V_{BE} for $V_A = \infty$?

5.75. Recalculate the currents in the transistor in Fig. 5.16 if $\beta_{FO} = 50$ and $V_A = 50$ V.

5.76. Repeat Prob. 5.63 if $V_A = 50$ V and $V_{BE} = 0.7$ V.

5.9 Transconductance

5.77. What is the transconductance of an *npn* transistor operating at 350 K and a collector current of (a) 10 μA, (b) 100 μA, (c) 1 mA, and (d) 10 mA? (e) Repeat for a *pnp* transistor.

5.78. (a) What collector current is required for an *npn* transistor to have a transconductance of 25 mS at a temperature of 320 K? (b) Repeat for a *pnp* transistor. (c) Repeat parts (a) and (b) for a transconductance of 40 μS.

5.10 Bipolar Technology and SPICE Model

5.79. (a) Find the default values of the following parameters for the generic *npn* transistor in the version of SPICE that you use in class: IS, BF, BR, VAF, VAR, TF, TR, NF, NE, RB, RC, RE, ISE, ISC, ISS, IKF, IKR, CJE, CJC. (*Note:* The values in Table 5.P1 may not agree exactly with your version of SPICE.) (b) Repeat for the generic *pnp* transistor.

5.80. A SPICE model for a bipolar transistor has a forward knee current IKF = 10 mA and NK = 0.5. How much does the KBQ factor reduce the collector current of the transistor in the forward-active region if i_F is (a) 1 mA? (b) 10 mA? (c) 50 mA?

5.81. Plot a graph of KBQ versus i_F for an *npn* transistor with IKF = 40 mA and NK = 0.5. Assume forward-active region operation with VAF = ∞.

5.11 Practical Bias Circuits for the BJT

Four-Resistor Biasing

5.82. (a) Find the Q-point for the circuit in Fig. P5.82(a). Assume that $\beta_F = 50$ and $V_{BE} = 0.7$ V. (b) Repeat the calculation if all the resistor values are decreased by a factor of 5. (c) Repeat if all the resistor values are increased by a factor of 5. (d) Find the Q-point in part (a) using the numerical iteration method if $I_S = 0.5$ fA and $V_T = 25.8$ mV.

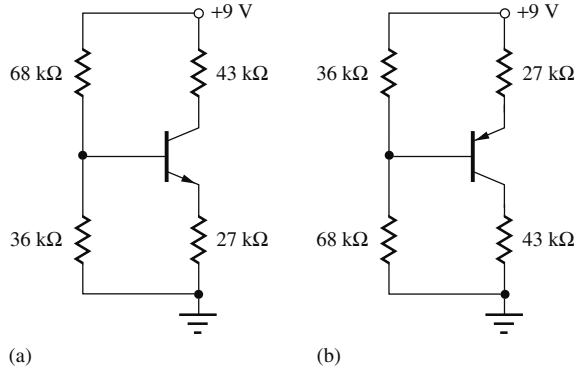


Figure P5.82

5.83. (a) Find the Q-point for the circuit in Fig. P5.82(a) if the 27-kΩ resistor is replaced with a 33-kΩ resistor. (b) Assume that $\beta_F = 75$.

5.84. (a) Find the Q-point for the circuit in Fig. P5.82(b). Assume $\beta_F = 50$ and $V_{BE} = 0.7$ V. (b) Repeat if all the resistor values are decreased by a factor of 5. (c) Repeat if all the resistor values are increased by a factor of 5. (d) Find the Q-point in part (a) using the numerical iteration method if $I_S = 0.4$ fA and $V_T = 25.8$ mV.

5.85. (a) Find the Q-point for the circuit in Fig. P5.82(b) if the 27-kΩ resistor is replaced with a 33-kΩ resistor. Assume $\beta_F = 75$ and $V_{BE} = 0.7$ V. (b) Repeat if all the resistor values are decreased by a factor of 5. (c) Repeat if all the resistor values are increased by a factor of 5. (d) Find the Q-point in part (a) using the numerical iteration method if $I_S = 1$ fA and $V_T = 25.8$ mV.

5.86. (a) Simulate the circuits in Fig. P5.82 and compare the SPICE results to your hand calculations of the Q-point. Use $I_S = 1 \times 10^{-16}$ A, $\beta_F = 50$, $\beta_R = 0.25$, and $V_A = \infty$. (b) Repeat for $V_A = 60$ V. (c) Repeat (a) for the circuit in Fig. 5.32(c). (d) Repeat (b) for the circuit in Fig. 5.32(c).

5.87. Find the Q-point in the circuit in Fig. 5.32 if $R_1 = 120$ kΩ, $R_2 = 270$ kΩ, $R_E = 100$ kΩ, $R_C = 150$ kΩ, $\beta_F = 100$, and the positive power supply voltage is 10 V.

5.88. Find the Q-point in the circuit in Fig. 5.32 if $R_1 = 6.2$ kΩ, $R_2 = 13$ kΩ, $R_C = 5.1$ kΩ, $R_E = 7.5$ kΩ, $\beta_F = 100$, and the positive power supply voltage is 15 V.

5.89. (a) Design a four-resistor bias network for an *npn* transistor to give $I_C = 10$ μA and $V_{CE} = 6$ V if $V_{CC} = 18$ V and $\beta_F = 75$. (b) Replace your exact values with the nearest values from the resistor table in Appendix C and find the resulting Q-point.

5.90. (a) Design a four-resistor bias network for an *npn* transistor to give $I_C = 1$ mA, $V_{CE} = 5$ V, and $V_E = 3$ V if $V_{CC} = 12$ V and $\beta_F = 100$. (b) Replace your exact values with the nearest values from the resistor table in Appendix C and find the resulting Q-point.

5.91. (a) Design a four-resistor bias network for a *pnp* transistor to give $I_C = 850$ μA, $V_{EC} = 2$ V, and $V_E = 1$ V if $V_{CC} = 5$ V and $\beta_F = 60$. (b) Replace your exact values with the nearest values from the resistor table in Appendix C and find the resulting Q-point.

5.92. (a) Design a four-resistor bias network for a *pnp* transistor to give $I_C = 11$ mA and $V_{EC} = 5$ V if $V_{RE} = 1$ V, $V_{CC} = -15$ V, and $\beta_F = 50$. (b) Replace your exact values with the nearest values from the resistor table in Appendix C and find the resulting Q-point.

Load Line Analysis

*5.93. Find the Q-point for the circuit in Fig. P5.93 using the graphical load-line approach. Use the characteristics in Fig. P5.26.

*5.94. Find the Q-point for the circuit in Fig. P5.94 using the graphical load-line approach. Use the characteristics in Fig. P5.26, assuming that the graph is a plot of i_C vs. v_{EC} rather than i_C vs. v_{CE}.

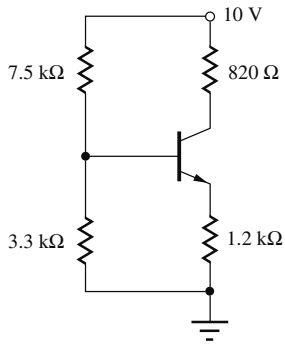


Figure P5.93

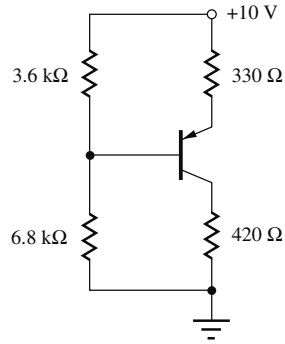


Figure P5.94

Bias Circuits and Applications

5.95. Find the Q-point for the circuit in Fig. P5.95 for (a) $\beta_F = 40$, (b) $\beta_F = 120$, (c) $\beta_F = 250$, (d) $\beta_F = \infty$. (e) Find the Q-point in part (a) using the numerical iteration method if $I_S = 0.5$ fA and $V_T = 25.8$ mV. (f) Find the Q-point in part (c) using the numerical iteration method if $I_S = 0.5$ fA and $V_T = 25.8$ mV.

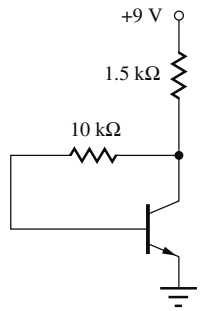


Figure P5.95

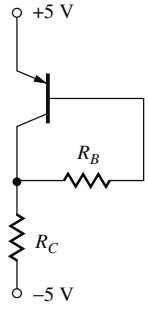


Figure P5.96

5.96. Design the bias circuit in Fig. P5.96 to give a Q-point of $I_C = 10$ mA and $V_{EC} = 3$ V if the transistor current gain $\beta_F = 60$. What is the Q-point if the current gain of the transistor is actually 40?

5.97. Design the bias circuit in Fig. P5.97 to give a Q-point of $I_C = 20$ μA and $V_{CE} = 0.90$ V if the transistor current gain is $\beta_F = 50$ and $V_{BE} = 0.65$ V. What is the Q-point if the current gain of the transistor is actually 125?

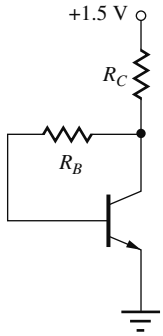


Figure P5.97

Bias Circuit Applications

5.98. The Zener diode in Fig. P5.98 has $V_Z = 6$ V and $R_Z = 100$ Ω. What is the output voltage if $I_L = 20$ mA? Use $I_S = 1 \times 10^{-16}$ A, $\beta_F = 50$, and $\beta_R = 0.5$ to find a precise answer.

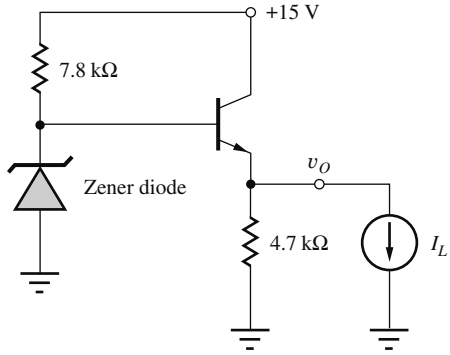


Figure P5.98

*5.99. Create a model for the Zener diode and simulate the circuit in Prob. P5.98. Compare the SPICE results to your hand calculations. Use $I_S = 1 \times 10^{-16}$ A, $\beta_F = 50$, and $\beta_R = 0.5$.

**5.100. The circuit in Fig. P5.100 has $V_{EQ} = 7$ V and $R_{EQ} = 100$ Ω. What is the output resistance R_o of this circuit for $i_L = 20$ mA if R_o is defined as $R_o = -dv_O/di_L$? Assume $\beta_F = 50$.

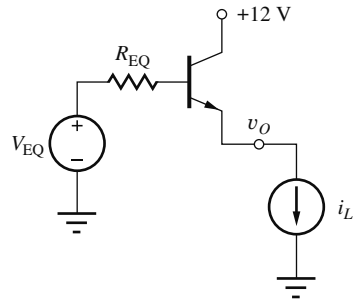


Figure P5.100

5.101. What is the output voltage v_O in Fig. P5.101 if the op-amp is ideal? What are the values of the base and emitter currents and the total current supplied by the 15-V source? Assume $\beta_F = 60$. What is the op-amp output voltage?

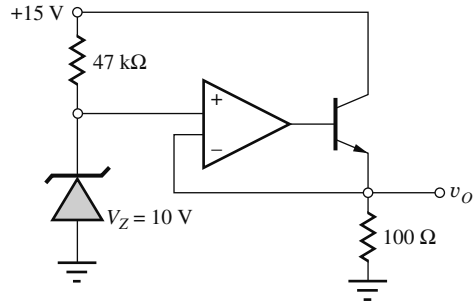


Figure P5.101

5.102. What is the output voltage v_O in Fig. P5.102 if the op-amp is ideal? What are the values of the base and emitter currents and the total current supplied by the 15-V source? Assume $\beta_F = 40$. What is the op-amp output voltage?

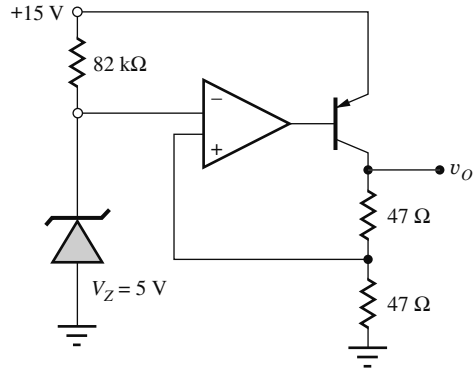


Figure P5.102

术语对照

Active region	有源区
Base	基极
Base current	基极电流
Base width	基区宽度
Base-collector capacitance	基极-集电区电容
Base-emitter capacitance	基极-发射区电容
Base-width modulation	基区宽度调制
β-cutoff frequency f_β	β截止频率 f_β
Bipolar junction transistor(BJT)	双极型晶体管（BJT）
Collector	集电极
Collector current	集电极电流
Common-base output characteristic	共基极输出特性
Common-emitter output characteristic	共发射极输出特性
Common -emitter transfer characteristic	共发射极转移特性
Cutoff region	截止区
Dc bias	直流偏置
Diffusion capacitance	扩散电容
Early effect	Early效应
Early voltage V_A	Early电压 V_A
Ebers-Moll model	EM模型
Emitter	发射极
Emitter current	发射极电流
Equilibrium electron density	平衡电子密度
Transfer characteristic	传输特性
Forward-active region	正向有源区
Forward common-emitter current gain β_F	正向共发射极电流增益β_F
Forward common-base current gain	正向共基极电流增益
Forward transit time τ_F	正向传输时间 τ_F
Forward transport current	正向传输电流
Gummel-Poon model	GP模型
Inverse-active region	反向有源区
Inverse common-emitter current gain	反向共发射极电流增益
Inverse common-base current gain	反向共基极电流增益

Monte Carlo analysis	蒙特卡洛分析
Normal- active region	正向有源区
Normal common-emitter current gain	共发射极电流增益
Normal common-base current gain	共基极电流增益
npn transistor	*npn*晶体管
Output characteristic	输出特性
pnp transistor	*pnp*晶体管
Quiescent operating point	静态工作点
Q-point	Q点
Reverse-active region	反向有源区
Reverse common-emitter current gain	反向共发射极电流增益
Reverse common-base current gain α_R	反向共基极电流增益 α_R
Reverse common-base current gain β_R	反向共发射极电流增益 β_R
Saturation region	饱和区
Saturation voltage	饱和电压
SPICE model parameters BF、IS、VAF	SPICE模型参数BF、IS、VAF
Transconductance	跨导
Transfer characteristic	转移特性
Transistor saturation current	晶体管饱和电流增益
Transport model	传输模型
Transistor Unity-gain frequency	电流增益频率
Unity-gain frequency f_T	单位增益频率 f_T
Worst-case analysis	最差情况分析