Chapter 5

CHAPTER 5

Comparator

With the rapid development of integrated circuit, the mixed-signal integrated system, especially the VLSI chip represented by System-On-Chip (SoC), has a large number of analog-to-digital converters, automatic gain control loops (AGC), peak detectors and other circuits. As a key module in these circuits, comparators have been an important circuit module in academia and industry. Their speed, power consumption, noise, offset voltage and other performances play a crucial role in the speed, accuracy and power consumption of the whole system.

5.1 Basis of comparator

The main function of comparator circuit is to compare an analog signal with another or reference signal, and output it to get the high and low voltage as binary signal through comparison processing. In the ideal case, when the difference between positive and negative inputs of comparator is positive, the output is high (V_{OH}). And when the input difference is negative, the comparator output is low (V_{OL}). The ideal transfer curve of comparator is shown in Fig. 5.1, where V_p is the inverse input, V_n is the inverse input. And the maximum and minimum value of comparator output is defined as V_{OH} and V_{OL} respectively. In practical circuit, V_{OH} and V_{OL} usually correspond to the power supply voltage and the ground voltage respectively.

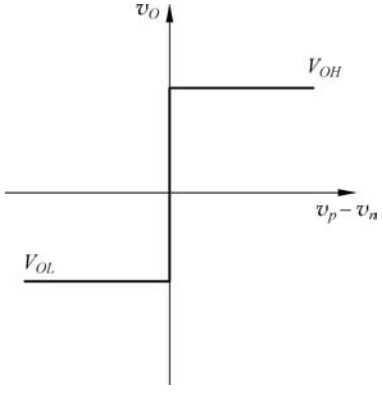

Fig. 5.1 The ideal transfer curve of comparator

When the voltage difference between two input is zero, the comparator output will not change. Actually comparators can not identify the tiny voltage difference without limitation. Due to the limitation of finite gain, there is usually a minimum resolvable voltage difference, which is called the accuracy (or resolution) of comparators. Figure 5.2 shows the transfer curve of a finite-gain comparator.

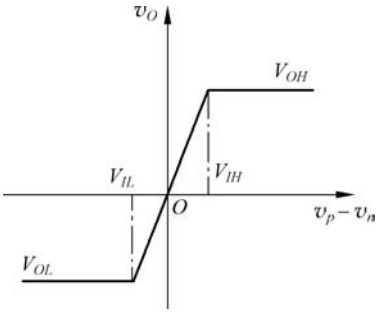

Fig. 5.2 The transfer curve of a finite-gain comparator

The V_{IH} and V_{IL} are the input voltage difference $V_p - V_n$ required by the output to reach the upper limit and the lower limit, which is the accuracy (resolution) of the comparator.

5.2 Parameter

The comparator parameters include two aspects of static and dynamic characteristics. The static characteristics include gain, resolution, offset voltage, etc. The dynamic characteristics mainly include the operating characteristics of small and large signals. The specific definitions of the various parameters are given below.

1. Resolution

Resolution is the minimum input voltage difference that can produce correct digital output. In some analog-to-digital converters, such as Flash ADC and successive approximation analog-to-digital converter, the comparator resolution directly determines the Effective Number Of Bit (ENOB) of ADC. The main factors affecting the resolution are noise, gain and the input offset voltage. The influence of offset voltage is the most serious, and it is mainly restricted by the CMOS technology. The definition is expressed:

$$\Delta V = \frac{V_{OH} - V_{OL}}{A_v} \tag{5-1}$$

where A_v is the comparator gain, that is the slope of transition curve, whose expression is

$$A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \tag{5-2}$$

2. Delay

The delay is generally defined as the time difference between the input analog signal

and the output digital signal. This parameter determines the maximum operating frequency of comparator.

3. Slew rate

The delay of comparator varies with the change of input amplitude, and the larger input will make the delay shorter. When the input is increased to an upper limit that will not affect the delay, the voltage change rate is called slew rate.

4. Kick-back noise

Kick-back noise refers to the noise generated by digital output to the input analog signal. The noise is usually caused by charge feedback.

5. V_{offset} (V_{OS})

The input offset voltage is produced by the mismatch of input differential MOS transistors or process. The MOS device shows a more serious input offset voltage than the BJT transistor. And the input offset voltage is also an important factor affecting the resolution of comparator. It is defined as: if the two input of comparator are connected to the same voltage value, the output is the offset voltage. The transfer curve of comparator introduced into the input offset voltage is shown in Fig. 5.3.

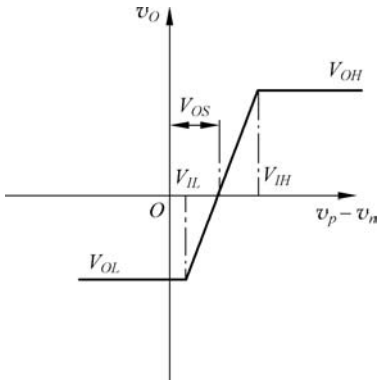

Fig. 5.3 The transfer curve of comparator introduced into the input offset voltage

6. Input common mode range

The input common mode range is the difference range of input voltage that the comparator can continuously distinguish. This characteristic is also one of the important characteristics of comparator.

7. Differential input voltage range

The differential input voltage range is defined as the maximum voltage allowed by the two input of comparator.

8. Output swing

The comparator outputs positive voltage when the inphase input voltage is greater than the negative input. The output swing is determined by the differential amplifier and the bias network within comparator, and it is also affected by the power supply voltage.

5.3 Characteristic analysis

The analysis of the comparator mainly divided into static and dynamic characteristic analysis. The following is the specific analysis.

1. Static characteristics analysis

The gain of the actual comparator is defined as $A_v = (V_{OH} - V_{OL})/V_{IH} - V_{IL}$, which is a finite value. V_{IH} and V_{IL} are the inphase and inverse input voltages required for the output to reach the upper and the lower limit. V_{OH} and V_{OL} are the output high and low voltage respectively. The gain is usually considered a function of its input signal. In structure, there are a variety of ways to improve its gain value. It is commonly used to add a or multi-stage pre-amplifier before the comparator; and add a inverter after the comparator to pull the output to the supply voltage or ground.

The resolution is the difference between the smallest input signal that the comparator can distinguish. It can be seen that the relationship between the resolution and the gain is very close, and the high resolution comparator circuit also means that its gain is higher.

The gain of an ideal comparator can be considered infinitely large, that is, when the input crosses zero, the output is changing. But the actual situation is that only when the input differential voltage reaches a certain voltage V_{OS}, the output starts to change. The voltage V_{OS} at this time is the input offset voltage. For the input offset voltage, the mismatch introduced in production process and the change of environment are the main reasons.

For the offset of technological deviation and environmental change, the magnitude of input offset voltage is often stochastic, and the polarity of its voltage is also unpredictable and drift along with temperature. In comparator circuit design, the impact of the offset voltage can be reduced by introducing an input or output offset storage technology.

In the common mode input range, the comparator input can be processed to output the right digital code, that is, the input transistors are in the normal operating state. At this point, the resolution and the input offset voltage can be considered as a function of the input common mode range.

2. Dynamic analysis

To analyze the dynamic characteristics, the small-signal and the large-signal characteristics of comparator will be discussed. First, when the input signal is small, the analysis is done by the small-signal analysis method. While the input signal increases, the delay decreases. Until the input amplitude increases to a certain extent, even if the input signal continues to increase, the delay will no longer change. The voltage change rate at this time is called Slew Rate (SR). As the input signal continues to increase, the

comparator eventually enters the large-signal mode. In these two operating mode, the determinants of comparator's delay are different. In general analysis, in small-signal mode, the larger input amplitude and higher gain will shorten the delay time.

For small-signal behavior, the delay is mainly caused by the nonlinear characteristics of circuit. For large-signal behavior, SR is mainly limited by the output driving capacity, which is shown as the charge and discharge speed of load capacitor. In comparator design, if the delay of jitter is required smaller, we should make SR a major determinant, and avoid the influence of zero/pole in signal frequency range. Then the delay can be expressed as

$$\tau_p = \frac{V_{OH} - V_{OL}}{2 \cdot SR} \tag{5-3}$$

Therefore, in order to reduce the delay, it is necessary to increase the current capacity and SR of comparator. It also means that there is a certain tradeoff between the power and speed.

5.4 Comparator structure

From the principle of operation, all comparators can be regarded as the different applications of amplifier. So it can be divided into two basic structures: open-loop and closed-loop. A high-gain OPA in open-loop state is a high-resolution comparator, and the hysteresis comparator and latch circuit is closed-loop amplifier with positive feedback.

From the aspect of power consumption, comparator includes static and dynamic comparator. The main difference between the two is that the static comparator consumes a certain static power. While the static power consumption of dynamic comparator is zero, and it only consumes the dynamic power dissipation.

According to the principle of operation, the comparator circuit can also be divided into the open-loop comparator and the regeneration comparator. Based on circuit structure, it consists of single-end output and differential-output structure. In design, it is more reasonable to choose the corresponding comparator circuit structure according to the application scene. The following is a brief introduction to open-loop comparator and dynamic comparator.

1. Open-loop comparator

The open-loop comparator is realized by open-loop amplifier. Such comparators do not need frequency compensation, so that the maximum bandwidth can be obtained. Meanwhile in theory, a relatively fast response time can be acquired. This comparator can be classified into a single-stage high-gain comparator and a low-gain multi-stage cascade comparator according to the amplifier structure.

The comparator formed by open-loop single-stage amplifier mainly depends on the amplifier's high-gain to enlarge the input differential signal to supply voltage and ground, so as to output digital code "1" and "0". This comparator does not have feedback

and circuit structure is simple. However, it can not be used in high-resolution systems because of its poor performance of offset voltage, setup time, and slew rate. And because the DC gain is high, and the bandwidth is small, the setup time is relatively long, which is generally suitable for single-pole system and small-signal input application.

Considering the setup time, if we want to increase the comparison speed, we need to increase the dominant pole frequency of amplifier and ensure its original unit gain bandwidth unchanged. This method usually sacrifices a certain DC gain. In order to compensate for the decrease of DC gain, multi low-gain amplifiers can be cascaded to form a comparator circuit.

2. Dynamic comparator

The dynamic comparator is mainly divided into the resistor-divider comparator, the differential-pairs comparator and the charge-distribution comparator. Other kinds of comparators are usually improved on the basis of these comparators.

The structure of resistor-divider comparator is shown in Fig.5.4. The transistors M1～M4 operates in the linear region, which is equivalent to the voltage-control resistor. It can adjust the threshold voltage of comparator by changing its resistance value, and the M5～M12 forms the latch. Assuming the length of M1～M4 are the same, and $W_A = W_2 = W_4$, $W_B = W_1 = W_3$, the threshold of comparator is

$$V_{\text{in}}^{+} - V_{\text{in}}^{-} = \frac{W_B}{W_A}(V_{\text{ref}}^{+} - V_{\text{ref}}^{-}) \tag{5-4}$$

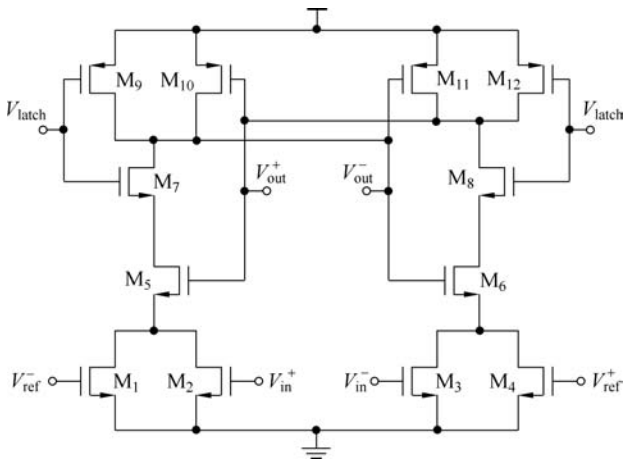

Fig. 5.4 The resistor-divider comparator

In this structure, the offset is mainly affected by M1～M4, and the effect of M5 and M6 on offset is relatively small. Because of the smaller size of transistors and the input transistors which have a large impact on offset operating in linear region, the structure has a larger offset. At the same time, since the large output changes has less effect on M1～M4 drain, this circuit is with low kick-back noise.

The differential-pairs comparator structure, as shown in Fig.5.5, is composed of two

cross-coupled differential pairs with a switch-controlled current source and a latch. The threshold can be set by introducing the imbalance of coupled pairs. Assuming that the length of M1 ~ M4 are equal and $W_1 = W_2$, $W_3 = W_4$, then the current of coupled pairs is expressed as

$$I_{D1} - I_{D2} = \beta_1 V_{\text{in}} \sqrt{\frac{2I_{D5}}{\beta_1} - V_{\text{in}}^2} \tag{5-5}$$

$$I_{D4} - I_{D3} = \beta_3 V_{\text{in}} \sqrt{\frac{2I_{D6}}{\beta_3} - V_{\text{ref}}^2} \tag{5-6}$$

where $\beta_i = (1/2)\mu C_{ox}(W_i/L)$, $V_{\text{in}} = V_{\text{in}}^+ - V_{\text{in}}^-$, $V_{\text{ref}} = V_{\text{ref}}^+ - V_{\text{ref}}^-$. When $I_1 = I_{D1} + I_{D3}$ equals $I_2 = I_{D2} + I_{D4}$, The state of comparator changes.

The offset voltage is mainly influenced by M1~M4. But its offset is smaller than the resistor-divider comparator. Unlike resistor-divider comparator, the large output changes has more effect on M1~M4 drain, so it generates high kick-back noise.

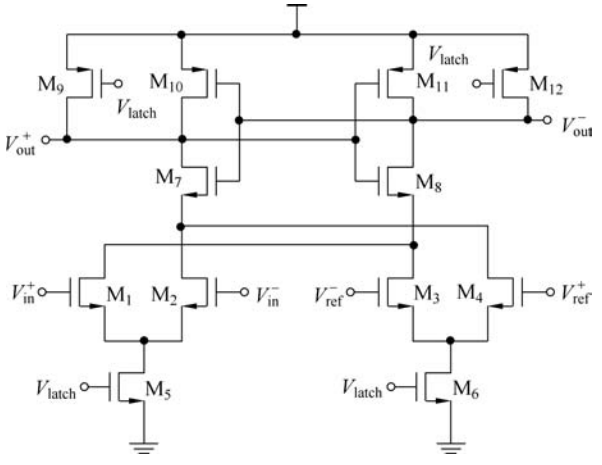

Fig. 5.5 The differential-pairs comparator

The charge-distribution comparator is demonstrated in Fig. 5.6. Its operating principle is as follows: when $\overline{\text{latch}}$ is high, the gate of M1 and M2 is connected to ground. C_{in} and C_{ref} are charged by V_{in}^- and V_{ref}^- respectively. At this time, the charge in C_{in} is $Q_{in} = V_{in} \cdot C_{in}$, and C_{ref} is $Q_{ref} = V_{ref} \cdot C_{ref}$. Since latch is low, M3 is cut-off, and M6、M9 turns on, which set V_{out}^- and V_{out}^+ as VDD and the latch circuit keeps the value of last judge. Meanwhile, M4 and M5 turns on that connects the drain of M1、M2 to VDD. After that latch changes to high, the bottom plate of C_{in} and C_{ref} connects to ground. According to the principle of conservation of charge:

$$V_{in}^- \cdot C_{in} + V_{ref}^- \cdot C_{ref} = V_- \cdot (C_{in} + C_{ref}) \tag{5-7}$$

$$V^- = V_{in}^- \frac{C_{in}}{C_{in} + C_{ref}} + V_{ref}^- \frac{C_{ref}}{C_{in} + C_{ref}} \tag{5-8}$$

When latch is high, the gate voltage of M1 is:

$$V^+ = V_{in}^+ \frac{C_{in}}{C_{in} + C_{ref}} + V_{ref}^+ \frac{C_{ref}}{C_{in} + C_{ref}} \tag{5-9}$$

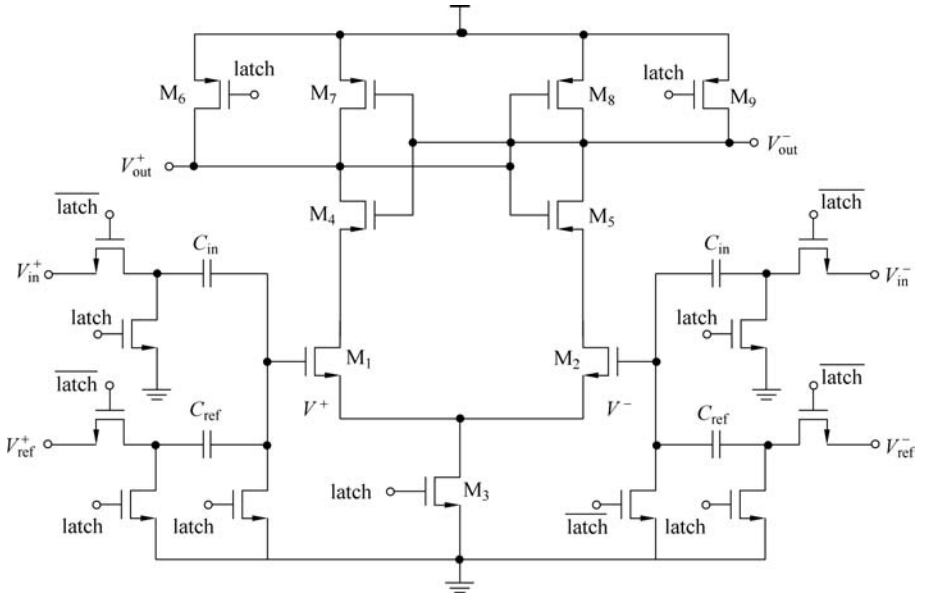

Fig. 5.6 The charge-distribution comparator

the input differential voltage of M1, M2 is:

$$V = V_{in}\frac{C_{in}}{C_{in}+C_{ref}} - V_{ref}\frac{C_{ref}}{C_{in}+C_{ref}} \tag{5-10}$$

where $V_{in} = V_{in}^{+} - V_{in}^{-}$, $V_{ref} = V_{ref}^{+} - V_{ref}^{-}$. At this moment, M3 turns on, and the gate voltage difference between M1 and M2 causes their drain to generate voltage difference, so that the flip flops composed of M4～M7 turn over and output signals. From the above analysis, when the differential input voltage is zero, the comparator start to work, thus the threshold is

$$V_{TH} = -V_{ref}\frac{C_{ref}}{C_{in}} \tag{5-11}$$

By setting the ratio of C_{in} and C_{ref}, the threshold of comparator can be adjusted. The offset of the structure is mainly determined by the mismatch of input differential pairs and the deviation of capacitance ratio. Besides kick-back noise, the error in the input switches is caused by charge injection.

The performance of these three kinds of dynamic comparator circuits is compared in Table 5.1.

Table5.1 Performance comparison

Category	Offset	Kick-back noise	Speed	Area	Power
the resistor-divider	large	small	slow	small	small
The differential-pairs	small	large	fast	medium	medium
The charge-distribution	small	medium	large	large	large

5.5 Basis of schmitt trigger

Schmitt trigger is actually a special comparator circuit that contains positive feedback. For standard Schmitt trigger, when the input voltage is higher than the forward threshold, the output is high; when the input voltage is below the negative threshold, the output is low; while the input is between positive and negative threshold, the output will not change. That is, when the output turns from high to low, or from low to high, the threshold is different. The output will change only when the input voltage varies enough, so this circuit is named as a trigger. This double-threshold action is called hysteresis, indicating the memory of Schmidt trigger. In essence, Schmitt trigger can be considered a bistable multivibrator.

Schmitt trigger can be used as a waveform shaping circuit to shape the analog signal waveform into square wave that the digital circuit can handle. Moreover, because Schmitt trigger has hysteretic characteristics, its applications include anti-disturbance in open-loop configuration, and realization of multivibrator in closed-loop positive feedback configuration. Schmidt trigger is divided into two kinds: non-reverse Schmidt trigger and reverse Schmidt trigger. The symbol and voltage transmission characteristics are shown in Fig.5.7(a) and(b).

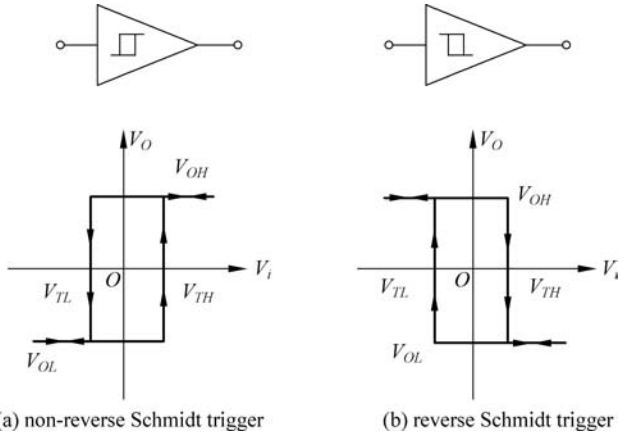

Fig. 5.7 The symbol and voltage transmission characteristics of two kinds of Schmidt trigger

In the discrete device system, Schmidt trigger circuit is usually built by an operational amplifier. In CMOS integrated circuits, Schmidt trigger are made up of only a few NMOS and PMOS transistors, a typical Schmidt trigger is shown in Fig.5.8. The Schmidt trigger contains two similar sub-circuit structures (M1, M2, M3 and M4, M5, M6). Each sub-circuit can be regarded as a nonlinear load of another sub-circuit. But when it is in the working state, that is, at the transition point, each of the sub-circuits can be regarded as the linear resistor load of the other sub-circuit.

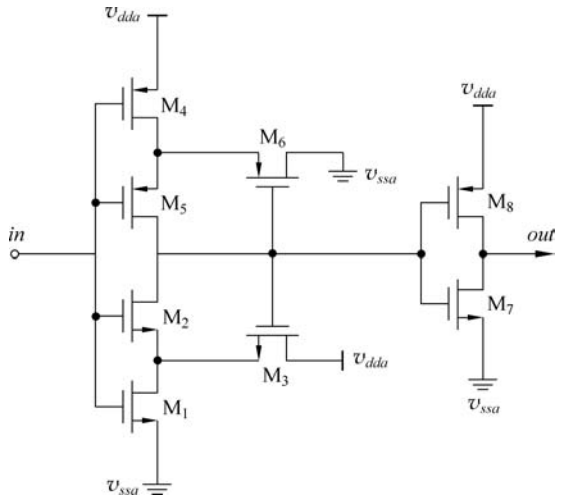

Fig. 5.8 Schmidt trigger

1. The current-voltage characteristics

In the circuit of Fig. 5.8, the bottom circuit M1, M2, M3 (which is called here the N-subcircuit), is loaded by the top circuit, M4, M5, M6 (P-subcircuit). To obtain the voltage-current characteristics of these nonlinear loads, one can take, for example, the N-subcircuit, apply a voltage source V_0, and calculate the source current I_0, assuming a constant voltage V_G at the gates of M1 and M2 (Fig. 5.9)

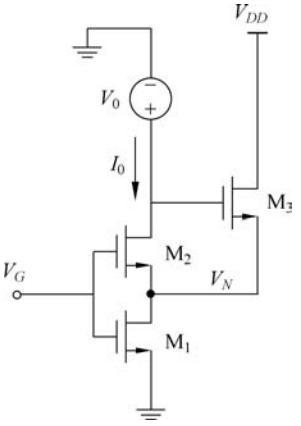

Fig. 5.9 Half equivalent circuit

When the voltage V_0 is very small, transistor M3 will be off, and M1 and M2 are in the triode mode of operation. The current I_0 is equal to

$$I_0 = 2k_1(V_G - V_{TN})V_N \tag{5-12}$$

where V_{TN} is the threshold of NMOS, $V_G - V_{TN}$ is the overdrive voltage. if one considers transistor M1, or:

$$I_0 = 2k_2(V_G - V_N - V_{TN})(V_0 - V_N) \tag{5-13}$$

In (5-12) and (5-13), it is assumed that $V_G > V_{TN}$, For the triode mode of

operation, $V_N \ll V_{TN}$, and (5-13) can be simplified to:

$$I_0 = 2k_2(V_G - V_{TN})(V_0 - V_{TN}) \tag{5-14}$$

so from(5-12) and (5-14), we can get:

$$V_N = V_0 \cdot \frac{k_2}{k_1 + k_2} \tag{5-15}$$

$$I_0 = \frac{2k_1k_2(V_G - V_{TN})}{k_1 + k_2} \cdot V_0 \tag{5-16}$$

from(5-16) the equivalent resistance is:

$$R_{LN} = \left[\frac{\partial I_0}{\partial V_0}\right]^{-1} = \frac{k_1^{-1} + k_2^{-1}}{2(V_G - V_{TN})} \tag{5-17}$$

It is seen from(5-15) and (5-17) that, in this part of the subcircuit operation, transistors M1 and M2 may be considered as a series connection of two resistors.

When V_0 increases, M2 enters into saturation. Then I_0 is determined, depending on the considered transistor, or by

$$I_0 = 2k_1[V_G - V_{TN} - (V_N/2)]V_N \tag{5-18}$$

or:

$$I_0 = k_2(V_G - V_N - V_{TN})^2 \tag{5-19}$$

from(5-18) and (5-19) one can find that

$$V_N = (V_G - V_{TN})\left(1 - \sqrt{\frac{k_1}{k_1 + k_2}}\right) \tag{5-20}$$

from (5-20) when the voltage V_0 achieves the value of $V_{0s} = V_G - V_{TN}$, the current I_0 becomes constant and equal to

$$I_{0N} = \frac{k_1k_2}{k_1 + k_2}(V_G - V_{TN})^2 \tag{5-21}$$

Yet, an additional increase of V_0 will gradually introduce some changes. When V_0 achieves the value of

$$V_{0T} = V_G - (V_G - V_{TN})\sqrt{\frac{k_1}{k_1 + k_2}} \tag{5-22}$$

Then transistor M3 will be turned on, V_N starts to increase again, and the current I_0 is diminishing. When V_0 becomes equal to

$$V_{0c} = V_G + (V_G - V_{TN})\sqrt{k_1/k_3} \tag{5-23}$$

transistor M2 will be completely turned off and I_0 becomes equal to zero. At this instant, voltage V_N will be equal to $V_N = V_G - V_{TN}$, and M1 is entering into saturation. Transistor M1 carries the current

$$I_N = k_1(V_G - V_{TN})^2 \tag{5-24}$$

which is completely intercepted by M3. Additional increase of V_0 up to V_{DD} does not bring any changes and completes the current-voltage characteristic of the N-subcircuit. The analysis of current-voltage characteristics of the N-subcircuit is shown in Fig. 5.10.

Now the design problem can be formulated graphically [Fig. 5.11]. Assuming that

the trigger transition from one stable state to another takes place when the gate voltage has a required threshold value V_H, and allowing a current ΔI to flow at this instant in the transistors M1, M2, M3, and M4, one has to find and superimpose the current-voltage characteristics of the two subcircuits so that only one unstable intersection point exists. A similar condition is then applied for another transition point, characterized by another required threshold voltage V_L. The characteristics shown in Fig. 5.10 help to analyze the trigger behavior near the transition point and to apply it to the circuit of Fig. 5.8.

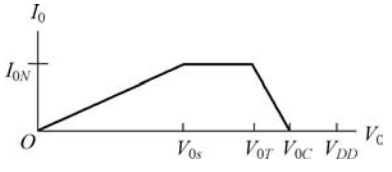

Fig. 5.10 current-voltage characteristics of the N-subcircuit

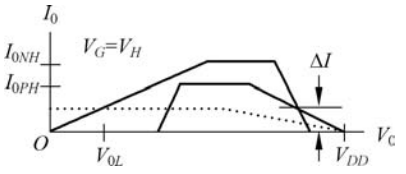

Fig. 5.11 The design problem

2. Threshold design

First it is assuming that the input $V_G = 0$ in Fig. 5.9. Then transistors M1 and M2 are off. Transistors M4 and Ms are in the linear mode of operation, but the voltage drop at each is zero because the current in M4 and Ms is equal to the current in M1 and M2. The output voltage V_0 is equal to V_{dd}. Transistor M3 is on (its drain and gate have the same voltage of V_{dd}) but it also does not carry any current.

When V_G rises above V_{TN}, transistor M1 turns on and starts to conduct. The current of M1 is determined by (5-24). It is completely intercepted by M3, and the condition of the transistors in the P-subcircuit does not change. However, the potential V_N is starting to decrease.

The trigger operation starts when the voltage V_G arrives at the value of V_{Hi}. At this point, due to simultaneous increase of V_G and decrease of V_N, transistor M2 turns on. It is not difficult to see that if in (5-23) one substitutes V_{dd} in stead of V_{0c} (the gate of M3 is still at V_{DD}) and V_{Hi} instead of V_G, one obtains the required relationship between the transistor parameters to start the triggering operation. It can be rewritten as

$$\frac{k_1}{k_3} = \left(\frac{V_{dd} - V_{Hi}}{V_{Hi} - V_{TNi}}\right)^2 \tag{5-25}$$

By the same reasoning, one obtains that the condition:

$$\frac{k_4}{k_6} = \left(\frac{V_{Li}}{V_{dd} - V_{Li} - |V_{TP}|}\right)^2 \tag{5-26}$$

The voltages V_{Hi} and V_{Li} considered as true thresholds of the CMOS Schmitt trigger. However, in effect, V_{Hi} and V_{Li} only function at the beginning of the triggering operation. The real triggering occurs at close but different voltages V_H and V_L. The difference depends on choice of the parameters k_2 and k_5, and can be estimated as follows.

The transition from one stable state to another in the Schmitt trigger is, indeed, very fast, and one can consider that during it the trigger input voltage does not change and

stays at V_H for the considered transition of the output voltage from high to low. When M2 is turned on, the trigger starts to operate as a linear circuit with positive feedback. Transistors M4 and M5 are in a linear mode of operation, and the trigger can be represented as the linear circuit shown in Fig. 5.12(a). The current of M1 is

$$I_{NH} = k_1 (V_H - V_{TN})^2 \approx k_1 (V_{Hi} - V_{TN})^2 \tag{5-27}$$

The trigger load is

$$R_{LP} = \frac{k_4^{-1} + k_5^{-1}}{2(V_{dd} - V_{Hi} - |V_{TP}|)} \tag{5-28}$$

The small-signal model for this part of trigger operation is shown in Fig. 5.12(b). The loop-transfer function for this circuit is

$$A_L = \frac{g_{m3} R_{LP} (g_{m2} r_{01} + 1)}{(g_{m2} + g_{m3}) r_{01} + 1} \tag{5-29}$$

where r_{01} is the output impedance of M1 that is operating in the saturation region.

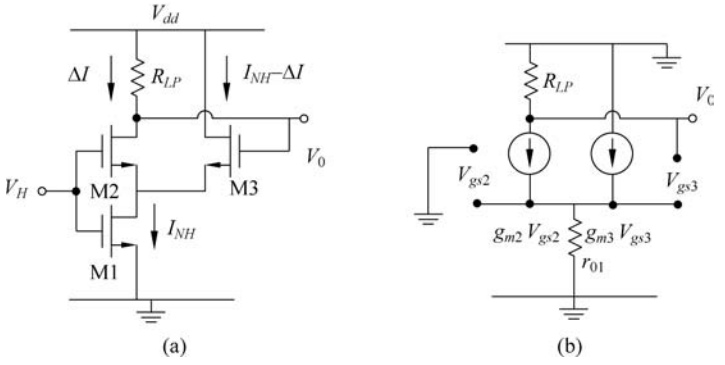

Fig. 5.12 Schmitt trigger during transition: (a) equivalent circuit and (b) small-signal model

At the moment of the output voltage jump from high to low, this loop transfer function becomes equal to unity. Assuming $g_{m2} r_{01} \gg 1$ and there is

$$\frac{R_{LP}}{g_{m2}^{-1} + g_{m3}^{-1} + (r_{01} g_{m2} g_{m3})^{-1}} = 1 \tag{5-30}$$

The current of M1 at this instant is divided between M2 and M3 into two parts ΔI and $I_{NH} - \Delta I$ so that the transconductance of the corresponding transistors are

$$g_{m2} = 2\sqrt{\Delta I \cdot k_2} \tag{5-31}$$

$$g_{m3} = 2\sqrt{(I_{NH} - \Delta I) \cdot k_3} \approx 2\sqrt{I_{NH} \cdot k_3} \tag{5-32}$$

the (5-30) can be simplified as:

$$g_{m2}^{-1} + g_{m3}^{-1} \approx R_{LP} \tag{5-33}$$

put (5-31) and (5-32) into (5-30), with (5-27) and (5-28) can get:

$$\Delta I = k_2^{-1} \left[\frac{k_4^{-1} + k_5^{-1}}{V_{dd} - V_{Hi} - |V_{TP}|} - \frac{1}{(V_{Hi} - V_{TN}) \sqrt{k_1 k_3}} \right]^{-2} \tag{5-34}$$

ΔI depends on k_2 and k_5. We can estimate the difference between V_{Hi} and V_H. In fact, when the transition starts one has the input voltage of V_H, transistor M2 has zero

current, transistor M3 carries the current of I_{NH}. and the trigger output voltage is equal to V_{dd}. Just before the output voltage jump, one has the input voltage of V_H, transistor M2 has the current of ΔI, M3 carries the current of $I_{NH}-\Delta I$, and the output voltage drops to $V_{dd}-\Delta IR_{LP}$. Using these conditions, it is easy to find that

$$\Delta V_H = V_H - V_{Hi} \approx \sqrt{\frac{\Delta I}{k_2}} - \Delta IR_{LP} \tag{5-35}$$

If transistor M3 is very wide we can use the approximation

$$\Delta I \approx \frac{(V_{dd} - V_{Hi} - |V_{TP}|)^2}{k_2(k_4^{-1} + k_5^{-1})^2} \tag{5-36}$$

if ΔIR_{LP} is neglected, put (5-36) into (5-35), finally we can obtain

$$\Delta V_H \approx \frac{V_{dd} - V_{Hi} - |V_{TP}|}{k_2 k_4^{-1} + k_2 k_5^{-1}} \tag{5-37}$$

Using the same method, considering the transition of the output voltage from low to high, we can get:

$$\Delta V_L \approx V_L - V_{Li} \approx -\frac{V_{Li} - V_{TN}}{k_5 k_2^{-1} + k_5 k_2^{-1}} \tag{5-38}$$

The values given by(5-37) and (5-38) can be considered as the worst case deflections of the thresholds. It is seen that to reduce ΔV_H and ΔV_L, the ratio k_2/k_5 should be kept constant and each of k_2/k_4 and k_5/k_1 should be increased simultaneously. Equations (5-37) and (5-38) provide necessary information for the CMOS Schmitt trigger design.

5.6 Technical words and phrases

5.6.1 Terminology

System-On-Chip(SoC)	片上系统
automatic gain control loops(AGC)	自动增益控制环路
peak detector	峰值检测器
resolution	分辨率
kick-back noise	回踢噪声
input common mode range	输入共模范围
output swing	输出摆幅
hysteresis comparator	迟滞比较器
latch	锁存器
Schmitt trigger	施密特触发器
bistable multivibrator	双稳态多谐振荡器

5.6.2 Note to the text

(1) The main function of comparator circuit is to compare an analog signal with another or reference signal, and output it to get the high and low voltage as binary signal

through comparison processing.

比较器电路的主要功能在于将一个模拟信号与另一个模拟信号或参考信号进行对比，并输出经过比较处理得到高低电平，作为二进制信号输出。

(2) Actually comparators can not identify the tiny voltage difference without limitation. Due to the limitation of finite gain, there is usually a minimum resolvable voltage difference, which is called the accuracy(or resolution) of comparators.

在实际电路中，比较器并不能无限制地分辨微小的电压差别，由于有限增益的限制，往往存在一个最小的可分辨电压差，这称为比较器的精度(或分辨率)。

(3) The delay is generally defined as the time difference between the input analog signal and the output digital signal. This parameter determines the maximum operating frequency of comparator.

传输延迟时间一般定义为输入模拟信号与输出数字信号之间的时间差。该参数决定了比较器的最高工作频率。

(4) It can be seen that the relationship between the resolution and the gain is very close, and the high resolution and high precision comparator circuit also means that its gain is higher.

由此可见，比较器的分辨率和增益之间的关系非常紧密，高分辨率高精度比较器电路也意味着其增益较高。

(5) A high-gain OPA in open-loop state is a high-resolution comparator, and the hysteresis comparator and latch circuit is closed-loop amplifier with positive feedback.

一个高增益的运算放大器工作于开环状态就是一个高分辨率的比较器，而迟滞比较器和锁存器电路则是带有正反馈的闭环放大器。

(6) The open-loop comparator is realized by open-loop amplifier. Such comparators do not need frequency compensation, so that the maximum bandwidth can be obtained. Meanwhile in theory, a relatively fast response time can be acquired.

开环比较器的特点是以放大器的开环应用作为基本比较器电路，这类比较器不需要频率补偿，从而可以获得尽可能大的带宽。理论上也就可以获得相对比较快的输出响应时间。

(7) This double-threshold action is called hysteresis, indicating the memory of Schmidt trigger. In essence, Schmitt trigger can be considered a bistable multivibrator.

这种双阈值动作被称为迟滞现象，表明施密特触发器有记忆性。从本质上来说，施密特触发器也可以认为是一种双稳态多谐振荡器。